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# User's Guide

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For Safety information, Warranties, and Regulatory information, see the pages behind the index.

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## Solutions for the Hitachi SH7750

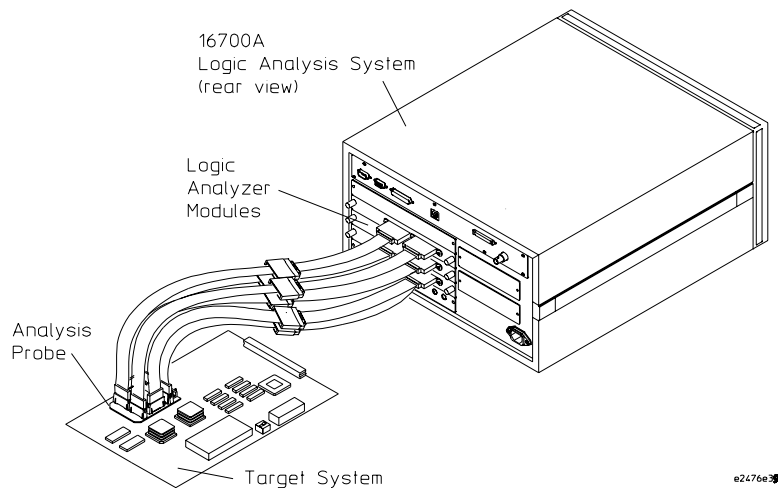
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## Solutions for the Hitachi SH7750—At a Glance

This manual describes several ways to connect an Agilent Technologies logic analyzer system to your target system. These connections use an analysis probe (or custom probing), plus an emulation module (for an emulation solution).

### Analysis Probe

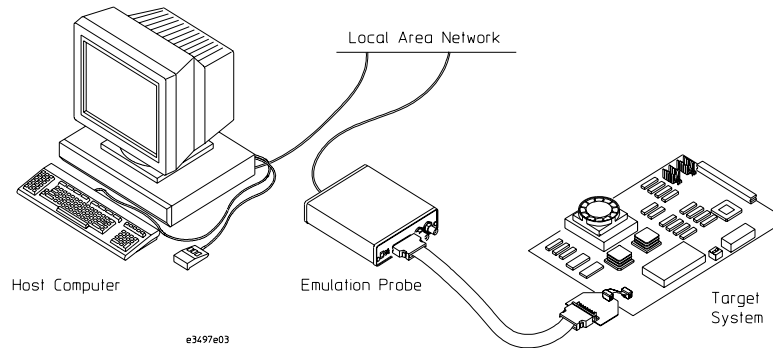
The analysis probe connects your logic analyzer to your target system for state and timing analysis. The analysis probe can be used with an Agilent Technologies 16600A/700A-series logic analyzer system. The analysis probe can be purchased alone, or as part of an emulation solution.



If your target system has the appropriate connectors, you can connect the logic analyzer directly to the target system and use the emulation solution user interface software without the analysis probe.

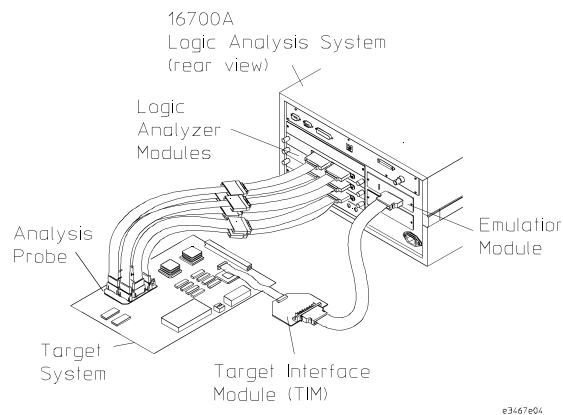
## Emulation Module

The emulation module plugs into your Agilent Technologies 16600A/700A-series logic analysis system frame. The emulation modules lets you use the target processor's built-in background debugging features, including run control and access to registers and memory. A high-level source debugger can use the emulation module to debug code running on the target system. You can connect the emulation module to the analysis probe or you can connect it to a debug port on the target system through the provided target interface module (TIM).



## Emulation Solution

The emulation solution includes an analysis probe, an emulation module, cables and adapters, and the Agilent Technologies B3759A Emulation Solution User interface software (For analyzing high-level code). This solution is designed to be used with an Agilent Technologies 16600A/700A-series logic analysis system.



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## In This Book

This book documents the following products:

### Analysis Probe

Processors supported	Agilent Technologies Product ordered	Includes
SH7750	E9598A	E8029A QFP analysis probe and E5346A high density adaptor cables

### Emulation Solution

Processors supported	Agilent Technologies Product ordered	Includes
SH7750	E9498A	E8029A QFP analysis probe, 16610A emulation module, E3467A target interface module (TIM), B3759A #710 Emulation Solution User Interface

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## Overview

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# Overview

This chapter describes:

- Setup Checklist
- Equipment used with the emulation probe
- Connection sequences for the emulation probe
- Equipment used with the emulation module
- Additional information sources

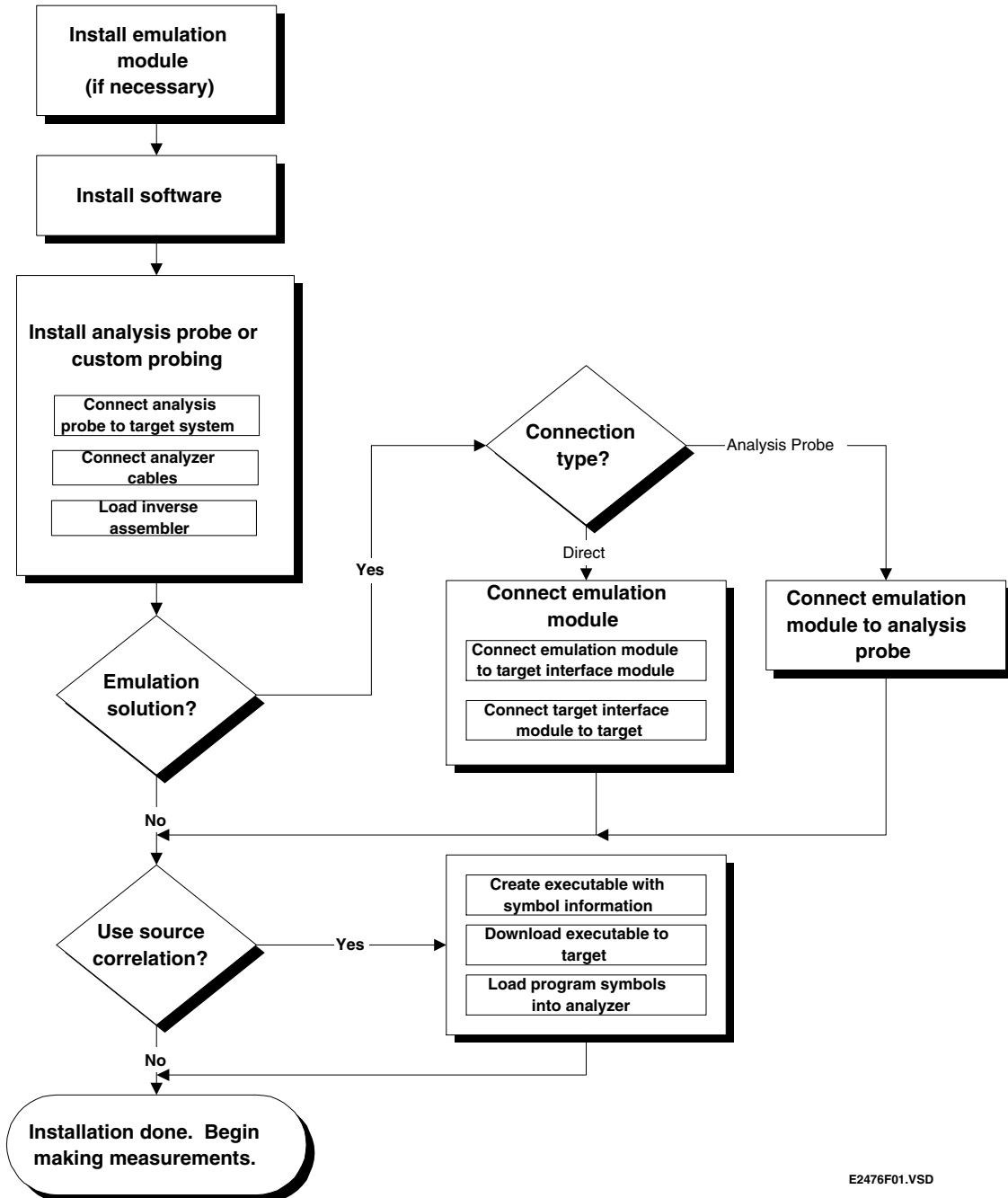
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## Setup Checklist

Follow these steps to connect your equipment:

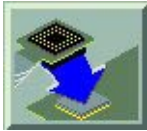
- Check that you received all of the necessary equipment. See pages 16 and 21.
- If you need to install an emulation module in an Agilent Technologies 16600A/700A series logic analysis system, see page 57.
- Install the software. See page 15.
- Use the Setup Assistant to help you connect and configure the analysis probe and emulation module. See page 15.

## Setup Flowchart



E2476F01.VSD

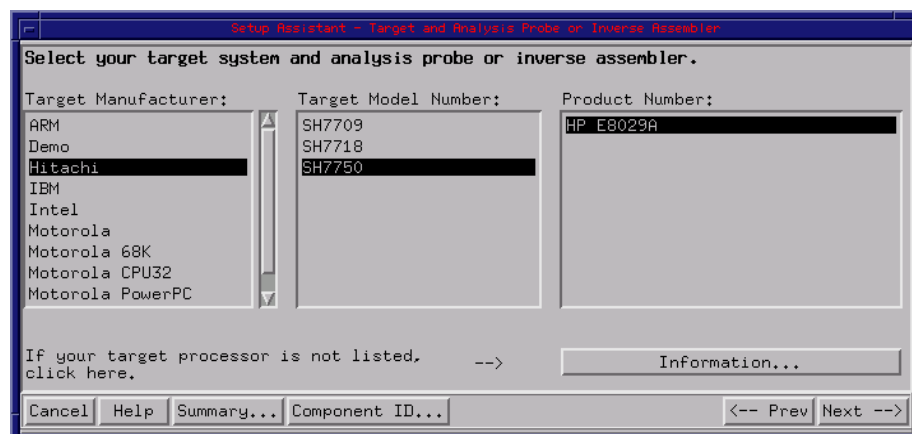
## Setup Assistant



The Setup Assistant is an online tool for connecting and configuring your logic analysis system for microprocessor and bus analysis. The Setup Assistant is available on the Agilent Technologies 16600A and 16700A-series logic analysis systems. You can use the Setup Assistant in place of the connection and configuration procedures provided in this manual.

This menu-driven tool will guide you through the connection procedures for connecting the logic analyzer to an Analysis Probe, an emulation module, or other supported equipment. It will also guide you through connecting an Analysis Probe to the target system.

Start the Setup Assistant by clicking its icon in the system window.



If you ordered this Analysis Probe or emulation solution with your Agilent Technologies 16600A/700A-series logic analysis system, the logic analysis system has the latest software installed, including support for this product. If you received this product after you received your logic analysis system, see the "Installing Software" chapter.

## Analysis Probe

This section lists equipment supplied with the analysis probe and equipment requirements for using the analysis probe.

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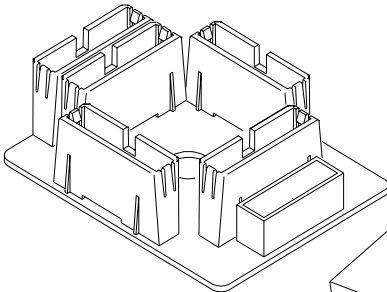
### Equipment supplied

The equipment supplied with the analysis probe is shown in the illustration on the next page. It is listed below.

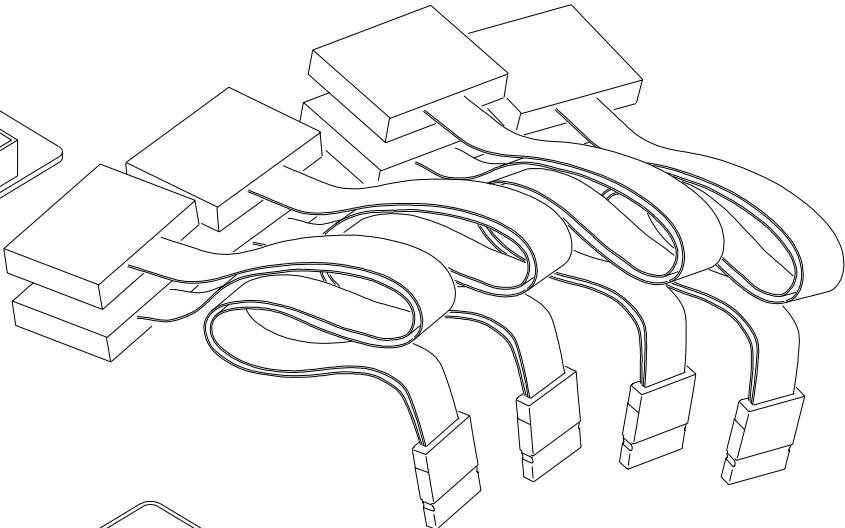
- Agilent Technologies E8029A analysis probe circuit board.
- An elastomeric probe adaptor.
- A retainer kit.
- Three Agilent Technologies E5346A high-density adaptor cables.
- Logic analyzer configuration files on a CDROM (for Agilent Technologies 16600A/700A series logic analysis systems).
- This User's Guide



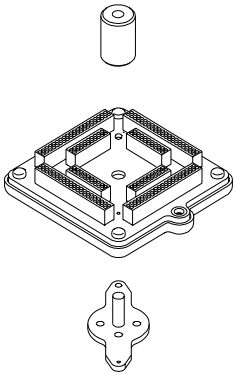
Analysis Probe



High-Density Termination Cables

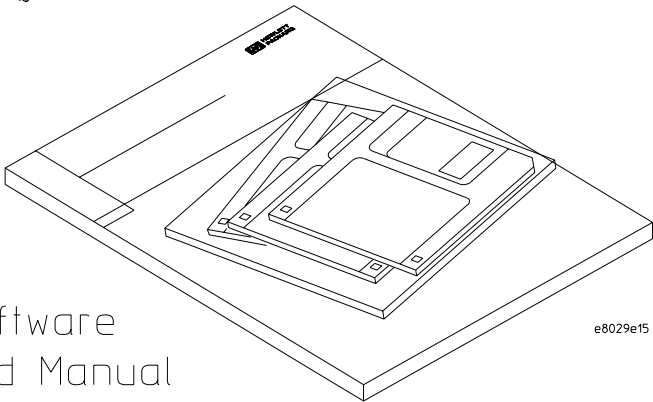


Elastomeric Probe Adapter



Pry Tool

Software and Manual



e8029e15

**Equipment Supplied with the Agilent Technologies E8029A Analysis Probe**

## Minimum equipment required

For state and timing analysis of an SH7750 target system, you need all of the following items.

- The Agilent Technologies E8029A Analysis Probe.
  - One of the logic analyzers listed on page 19.
- 

## Additional equipment supported

### **Emulation module**

The Agilent Technologies E8029A has a built-in connector for an Agilent Technologies 16610A emulation module.

### **Agilent Technologies B3759A #710 Interface Software**

The interface software can be used with the analysis probe to control your logic analyzer and inverse assembly of the trace result.

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## Logic analyzers supported

The table below lists the logic analyzers supported by the Agilent Technologies E8029A analysis probe and B3759A #710 interface software. Logic analyzer software version requirements are shown on the following page.

The Agilent Technologies E8029A and B3759A #710 require minimum of eight logic analyzer pods (136 channels) for inverse assembly.

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### Logic Analyzers Supported

Logic Analyzer	Channel Count	State Speed	Timing Speed	Memory Depth
16600A	204	100 MHz	125 MHz	64k states
16601A	136	100 MHz	125 MHz	64k states
16550A (two cards)	102/card	100MHz	250MHz	4k states
16710A (two cards)	102/card	100MHz	250MHz	8k states
16711A (two cards)	102/card	100MHz	250MHz	32k states
16712A (two cards)	102/card	100MHz	250MHz	128k states
16555A (two cards)	68/card	110MHz	250MHz	1M states
16555D (two cards)	68/card	110MHz	250MHz	2M states
16556A (two cards)	68/card	100MHz	200MHz	1M states
16556D (two cards)	68/card	100MHz	200MHz	2M states
16557D (two cards)	68/card	135MHz	250MHz	2M states

## Logic analyzer software version requirements

The logic analyzer must have the latest software to make a measurement with the Agilent Technologies E8029A. The latest Agilent Technologies 16600A/16700A logic analyzer software version is on the CDROM shipped with this product.

## Emulation Module

This section lists equipment supplied with the emulation module and lists the minimum equipment required to use the emulation module.

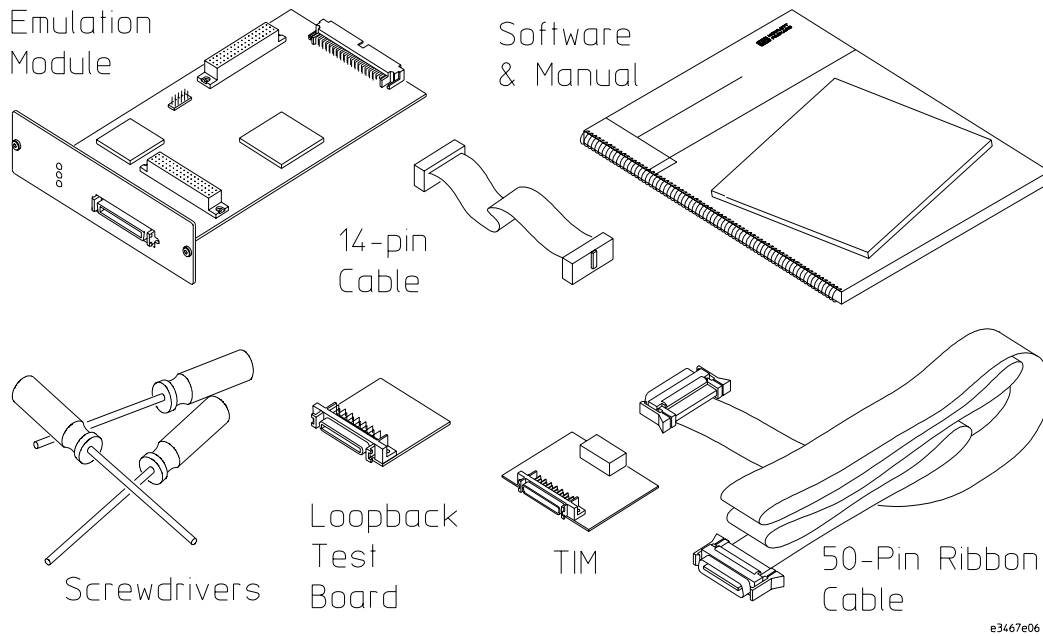
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### Equipment supplied

The equipment supplied with your emulation module includes:

- An Agilent Technologies 16610A emulation module. If you ordered an emulation module as part of your Agilent Technologies 16600A or 16700A logic analysis system, it is already installed in the frame.
- A target interface module (TIM) circuit board.
- A emulation module loopback test board (Agilent part number E3496-66502).
- Firmware for the emulation module on a CD-ROM.
- A 50-pin ribbon cable for connecting the emulation module to the target interface module.
- A 14-pin ribbon cable for connecting the target interface module to the target system.
- One Torx T-8, one Torx T-10, and one Torx T-15 screwdriver (if the emulation module was not installed at the factory).
- This User's Guide.

## Chapter 1: Overview Emulation Module



### Equipment Supplied with the Agilent Technologies E3497A Emulation Module

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#### Minimum equipment required

The following equipment is required to use the emulation module:

- A method for connecting to the target system. The Agilent Technologies E8029A analysis probe provides a debug port connector. You can also design a debug port connector on the target system.
- An Agilent Technologies 16600A or 16700A logic analysis system.
- A user interface on the host computer, such as B3759A#710 Emulation Solution Interface or 3rd party's high-level source debugger .

## Emulation Solution

An emulation solution uses the equipment and software already described in this chapter.

The combination of an analysis probe, an emulation module, and an Agilent Technologies 16600A or 16700A logic analysis system lets you both trace and control microprocessor activity on the target system.

The analysis probe supplies signals from the target microprocessor to the logic analyzer. A configuration file sets up the logic analyzer to properly interpret these signals.

You can use a Agilent Technologies B3759A #710 interface software to configure and control the target processor and to download program code.

## Additional Information Sources

Additional or updated information can be found in the following places:

Newer editions of this manual may be available. Contact your local Agilent Technologies representative.

If you have a probing adapter, the instructions for connecting the probe to your target microprocessor are in the **Probing Adapter** documentation.

Application notes may be available from your local Agilent Technologies representative or on the World Wide Web at:

**<http://www.agilent.com/find/logicanalyzer>**

If you have an Agilent Technologies 16600A or 16700A logic analysis system, the **online help** for the Emulation Control Interface has additional information on using the emulation module.

The **measurement examples** include valuable tips for making emulation and analysis measurements. You can find the measurement examples under the system help in your Agilent Technologies 16600A/700A logic analysis system.



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## Installing Software on a 16600A/700A

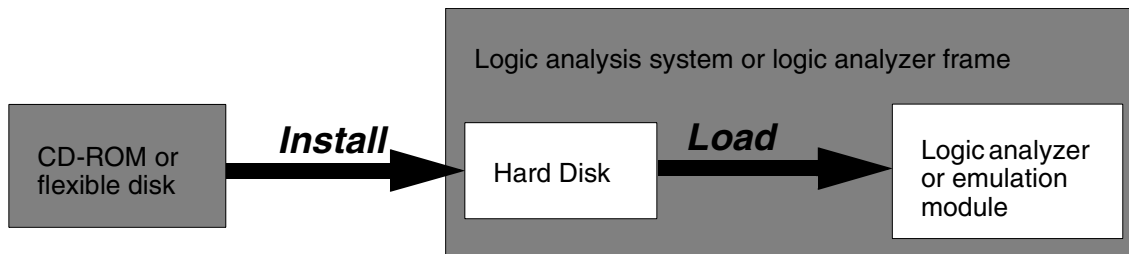
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## Installing Software on a 16600A/700A

This chapter explains how to install the software you will need for your analysis probe or emulation solution.

### **Installing and loading**

**Installing** the software will copy the files to the hard disk of your logic analysis system. Later, you will need to **load** some of the files into the appropriate hardware module.



## **What needs to be installed**

### **Agilent Technologies 16600A/700A-series logic analysis systems**

If you ordered an emulation solution with your logic analysis system, the software was installed at the factory.

The following files are installed when you install a processor support package from the CD-ROM:

- Logic analysis system configuration files
- Personality files for the Setup Assistant
- Emulation module firmware (for emulation solutions)
- Emulation Control Interface (for emulation solutions)

## To install the software from CD-ROM (16600A/700A)

Installing a processor support package from a CD-ROM will take just a few minutes. If the processor support package requires an update to the Agilent Technologies 16600A/700A operating system, installation may take approximately 15 minutes. If the CD-ROM drive is not connected, see the instructions printed on the CD-ROM package.

- 1 Turn on the CD-ROM drive first and then turn on the logic analysis system.
- 2 Insert the CD-ROM in the drive.
- 3 Click the **System Admin** icon.
- 4 Click **Install...** .  
Change the media type to "CD-ROM" if necessary.
- 5 Click **Apply**.
- 6 From the list of types of packages, select "PROC-SUPPORT."  
A list of the processor support packages on the CD-ROM will be displayed.
- 7 Click on the "sh4" package.  
If you are unsure if this is the correct package, click Details for information on what the package contains.
- 8 Click **Install...** .  
The dialog box will display "Progress: completed successfully" when the installation is complete.
- 9 Click **Close**.

The configuration files are stored in /hplogic/configs/hp/sh77xx/sh7750.

### See Also

The instructions printed on the CD-ROM package for a summary of the installation instructions.

The online help for more information on installing, licensing, and removing software.

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## Setting Up the Analysis Probe

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## Setting Up the Analysis Probe

This chapter shows you how to connect the logic analyzer to the target system through the analysis probe. If you are using custom probing, turn to page 48.

If you are connecting to an Agilent Technologies 16600A-series or 16700A series logic analyzer, use the Setup Assistant to connect and configure your system (see page 15). Use this manual for additional information, if desired.

If you are not using the Setup Assistant, follow the instructions given in this chapter. This chapter covers the following tasks; the order shown here is the recommended order for performing these tasks.

- Read the power on/off sequence
- Connect the analysis probe to the target system
- Connect the analysis probe to the logic analyzer

## Setting Up the Analysis Probe Hardware

Setting up the Analysis Probe hardware consists of the following major steps:

- Turn off the logic analyzer and the target system.
- Connect the Elastomeric Probing System retainer to the target system.
- Attach the Analysis Probe circuit board and adapter to the retainer.
- Attach the labels to the Agilent Technologies E5346A High-Density cables, then connect the cables to the Analysis Probe.
- Connect the logic analyzer pods to the high-density adapter cables.

The remainder of this section describes these general steps in more detail.

---

### Turn off the logic analyzer and the target system

To protect your equipment, remove the power from both the logic analyzer and the target system before you make or break connections. The logic analyzer should always be powered up before the target system. When powering down, power down the target system first and then power down the logic analyzer.

## To connect the Analysis Probe to the target system

Use the following steps to connect the Analysis Probe to the target system.

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### CAUTION

**Equipment Damage.** To prevent equipment damage, be sure to remove power from both the target system and the logic analyzer whenever the Analysis Probe is being connected or disconnected.

---

- 1 Turn off the target system and logic analyzer.**
- 2 Using the instructions in the *Agilent Technologies QFP Elastomeric Probing System Installation Guide*:**
  - Prepare to attach the Retainer to the QFP microprocessor
  - Test the alignment before adhering the Retainer
  - Adhere the Retainer to the QFP microprocessor
  - Install the Agilent Technologies E8029A Analysis Probe as described in "Install the Probe Adapter"
- 3 Using the illustration on the next page, note the following indicators:**
  - position of Pin 1 on the microprocessor
  - position of little pin on the retainer
  - position of little hole on the probe adapter

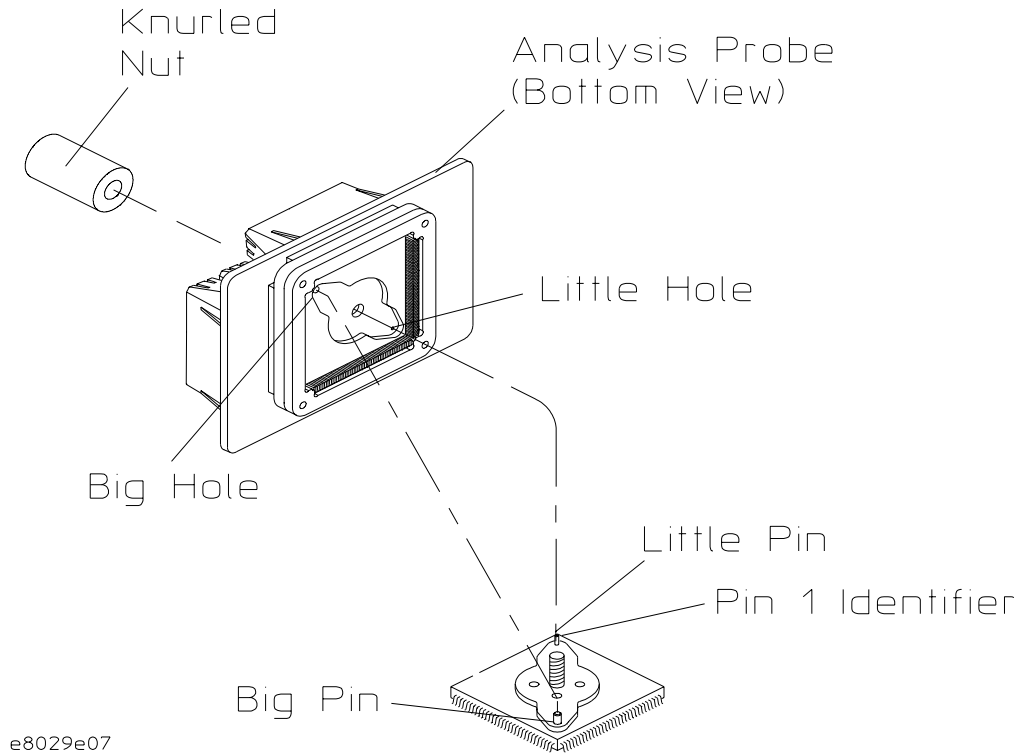
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### CAUTION

Serious damage to the target system or Analysis Probe can result from incorrect connection. Note the position of pin 1 on the target system and Analysis Probe prior to making any connection. Also, take care to align the pins so that all pins are making contact.

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#### Pin 1 Alignment for Target System and Analysis Probe

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### To disconnect the Analysis Probe from the target system

Use the following steps to disconnect the Analysis Probe from the target system.

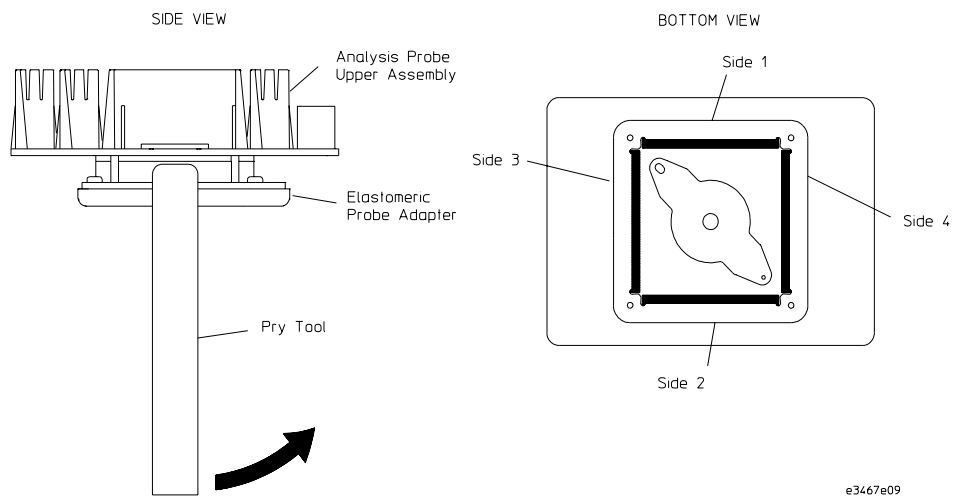
- 1 Remove power from the target system.**
- 2 Remove power from the logic analyzer.**
- 3 Unscrew the knurled nut.**
- 4 Lift the Analysis Probe straight up.**

---

## To separate the Analysis Probe upper assembly from the probe head

Agilent Technologies does not recommend separating the Analysis Probe upper assembly from the elastomeric probe head. However, unforeseen circumstances might require you to separate the assembly.

Use the Cam Tool supplied. Insert the tool into the first side as shown in the following illustration, and rotate it until the connectors begin to separate. Repeat this process for the other three sides in consecutive order until the Analysis Probe upper assembly and the elastomeric probe head are separated.



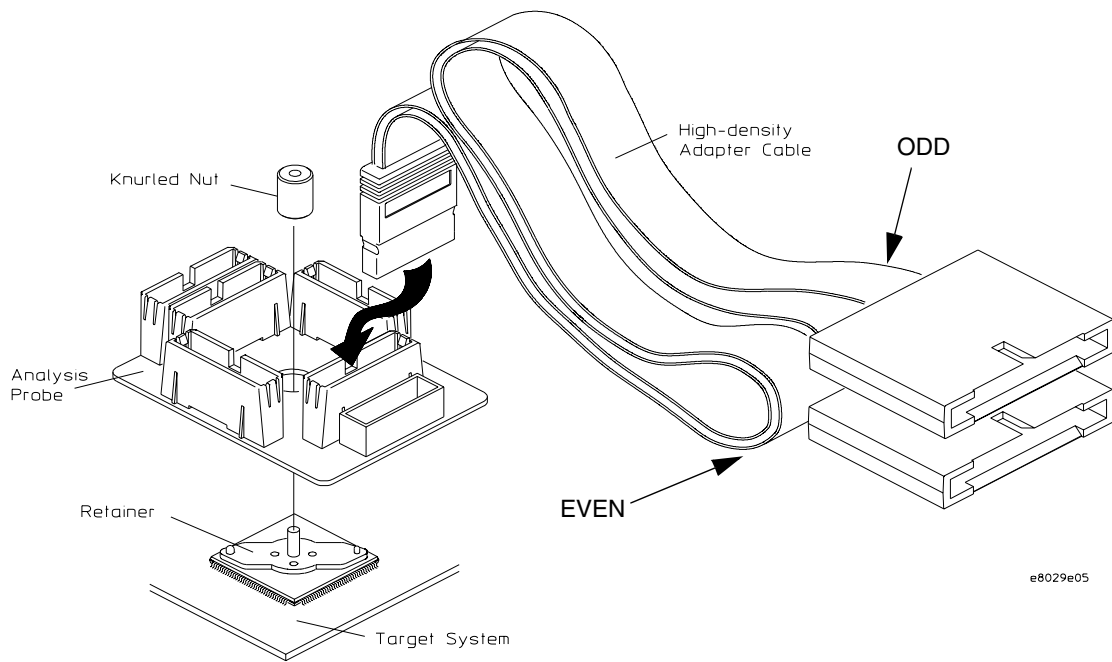
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## To reconnect Analysis Probe and probe head

Place the elastomeric probe head in its protective cover. Orient the elastomeric probe head and the Analysis Probe upper assembly as shown in the illustration on the previous page. As you begin to insert the pins of the Analysis Probe upper assembly into the sockets on the elastomeric probe head, ensure that all of the pins are engaging. Look closely at both ends of all four sockets to ensure all pins are properly mated. Gently apply pressure until the connectors are fully mated.

## To connect the high-density adapter cables to the Analysis Probe

The high-density adapter cables, and labels to identify them, are included with the Agilent Technologies E8029A Analysis Probe. The labels identify the cables by the pod number, and "o" or "e" (for odd or even). Attach the labels to the cables, then connect the cables to the connectors on the Analysis Probes as shown in the following illustrations.



### High-Density Adapter Cables

## Setting up the Logic Analyzer

Connect the logic analyzer pod cables to the logic analyzer and to the mictor connector on the Analysis Probe. Required number of pods depend on which memory type you are using, how many wait cycles are interleaved, and speed of your target system's CKIO speed. See table below, then refer to the pod diagram for the analyzer you are using.

External Bus Speed	Memory Types Combination		Description	POD	Minimum Logic Analyser supported	Config File	Type
	ROM, SRAM, BurstROM, or PCMCIA	Other memory					
<=40MHz (*1)(*2)	D.C.	D.C	Any memory combinations with external bus speed of 40MHz or slower	8	16601A	SH7750F_0	A
					16700A+16550Ax2	SH7750F_0	B
					16700A+16710/1/2x2	SH7750F_0	C
					16700A+16555/6/7x2(*2)	SH7750M_0	D
> 40MHz (*2)	YES	D.C	ROM, SRAM, PCMCIA , or BurstROM exist on your target system	10	16600A	SH7750F_1	E
					16700A+16550A	SH7750F_1	F
					16700A+16710/1/2x2	SH7750F_1	G
					16700+16555/6/7x3(*2)	SH7750M_1	H
	NO	YES	ROM, SRAM, PCMCIA, or BurstROM does not exist on your target system	8	16601A	SH7750F_0	A
					16700A+16550Ax2	SH7750F_0	B
					16700A+16710/1/2x2	SH7750F_0	C
					16700A+16555/6/7x2(*2)	SH7750M_0	D

D.C. = Don't Care

(\*1) Condition of <=40MHz : CKIO(cycle) = min25ns, CKIO(low)=min10ns, CKIO(high)=min10ns

(\*2) You may use any memory combinations under the bus speed of 50MHz using 16557.

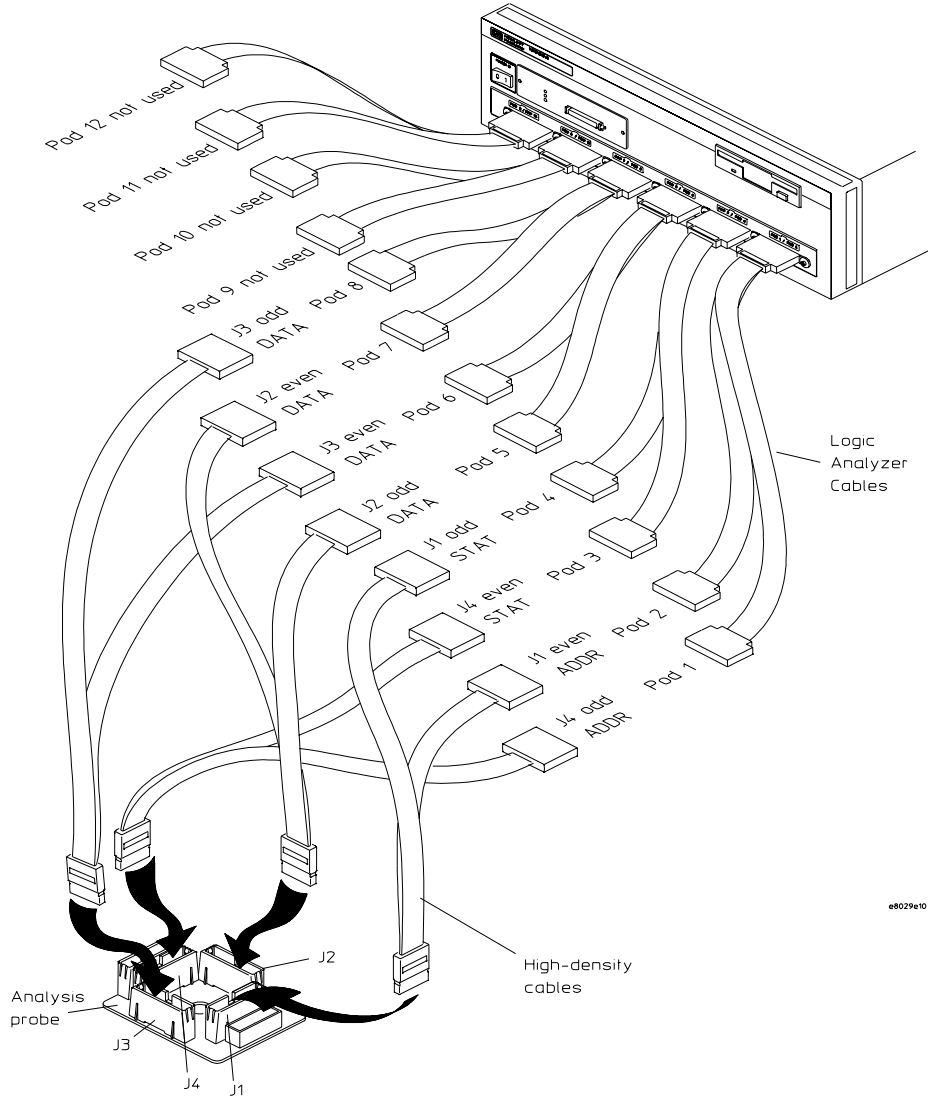
Condition of <=50MHz : CKIO(cycle) = min20ns, CKIO(low)=min7.5ns, CKIO(high)=min7.5ns

### Note

If your 16700A Logic Analyzer equips with three card analyzer (One master, and two slave modules) and your connection type is either "D", you must detach one of the slave module on your logic analyzer. (One master, and one slave) Refer to the analyzer manual for the instruction on how to detach the module.

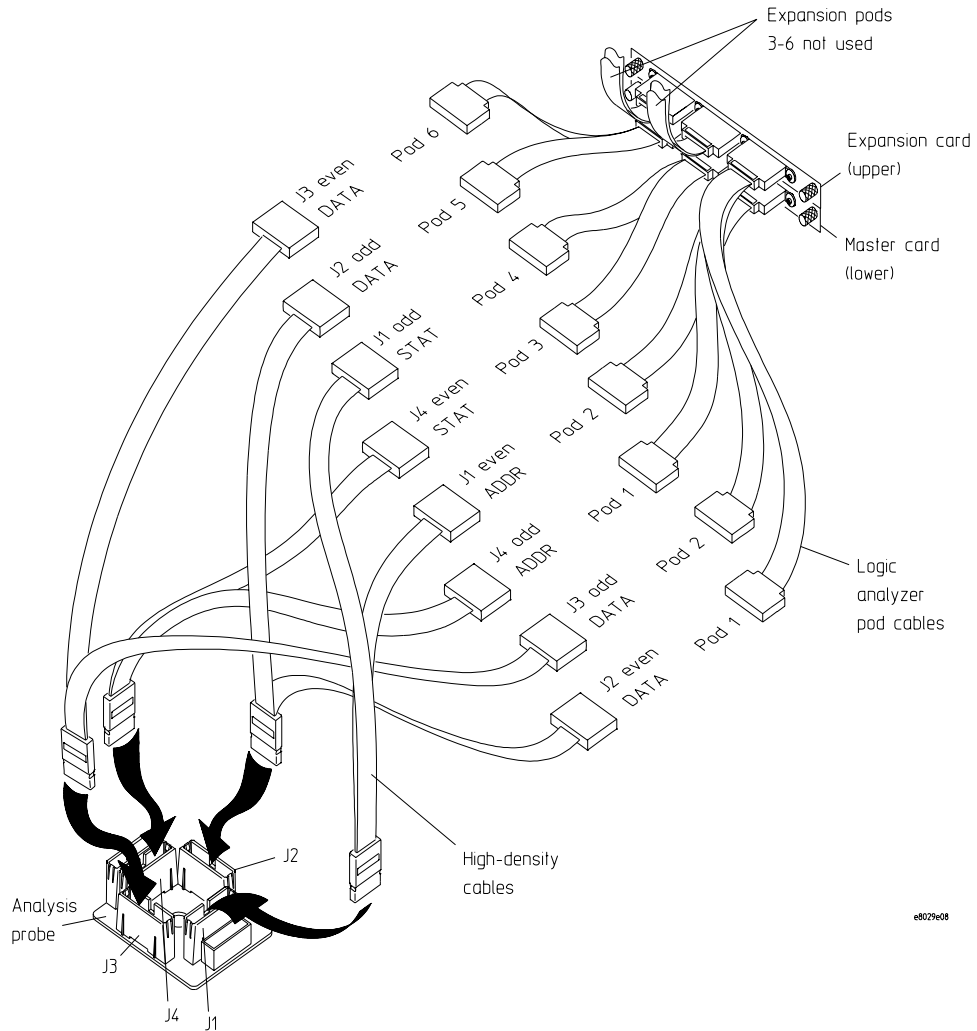
## Connection Type 'A' To connect to the 16600/1/2A analyzer

Connect the pod cables to the Analysis Probe according to the pod diagram below.



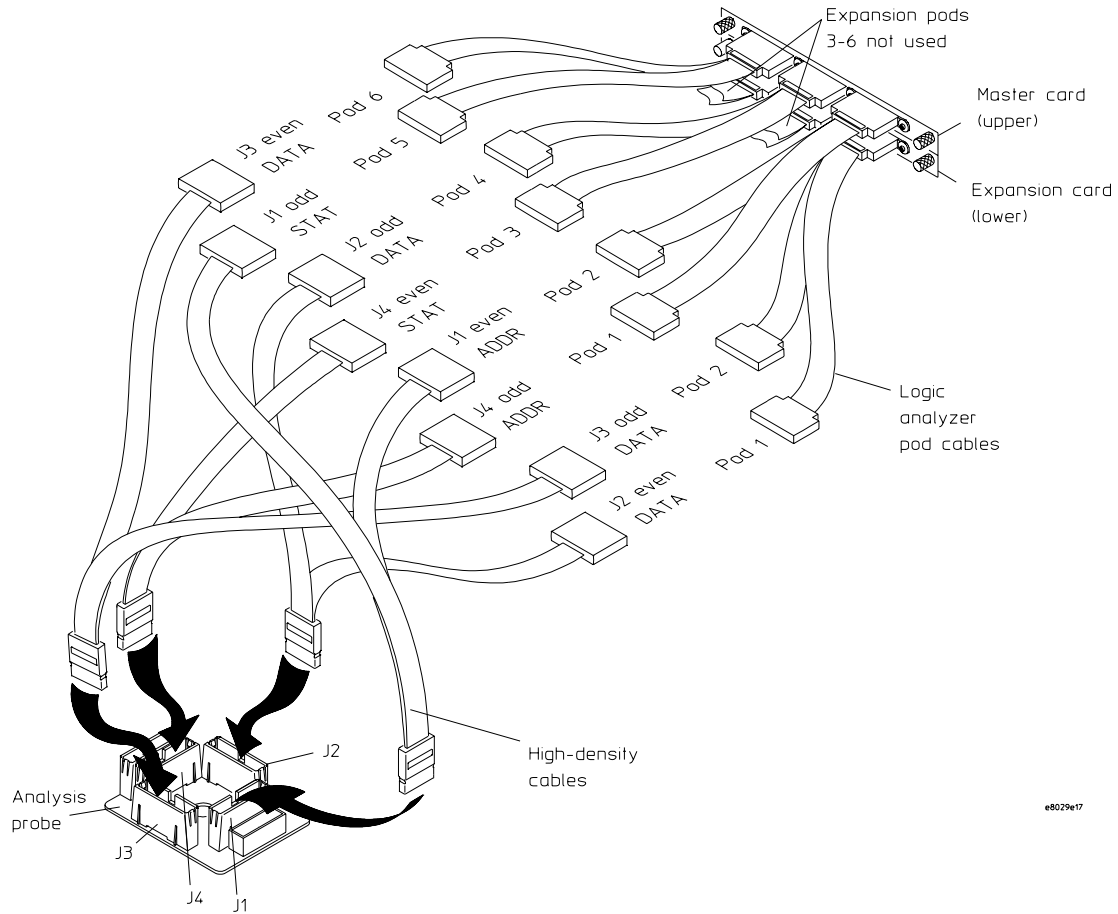
## Connection Type 'B' To connect to the 16550A two-cards analyzer

Connect the pod cables to the Analysis Probe according to the pod diagram below.



## Connection Type 'C' To connect to the 16710/1/2A two-cards analyzer

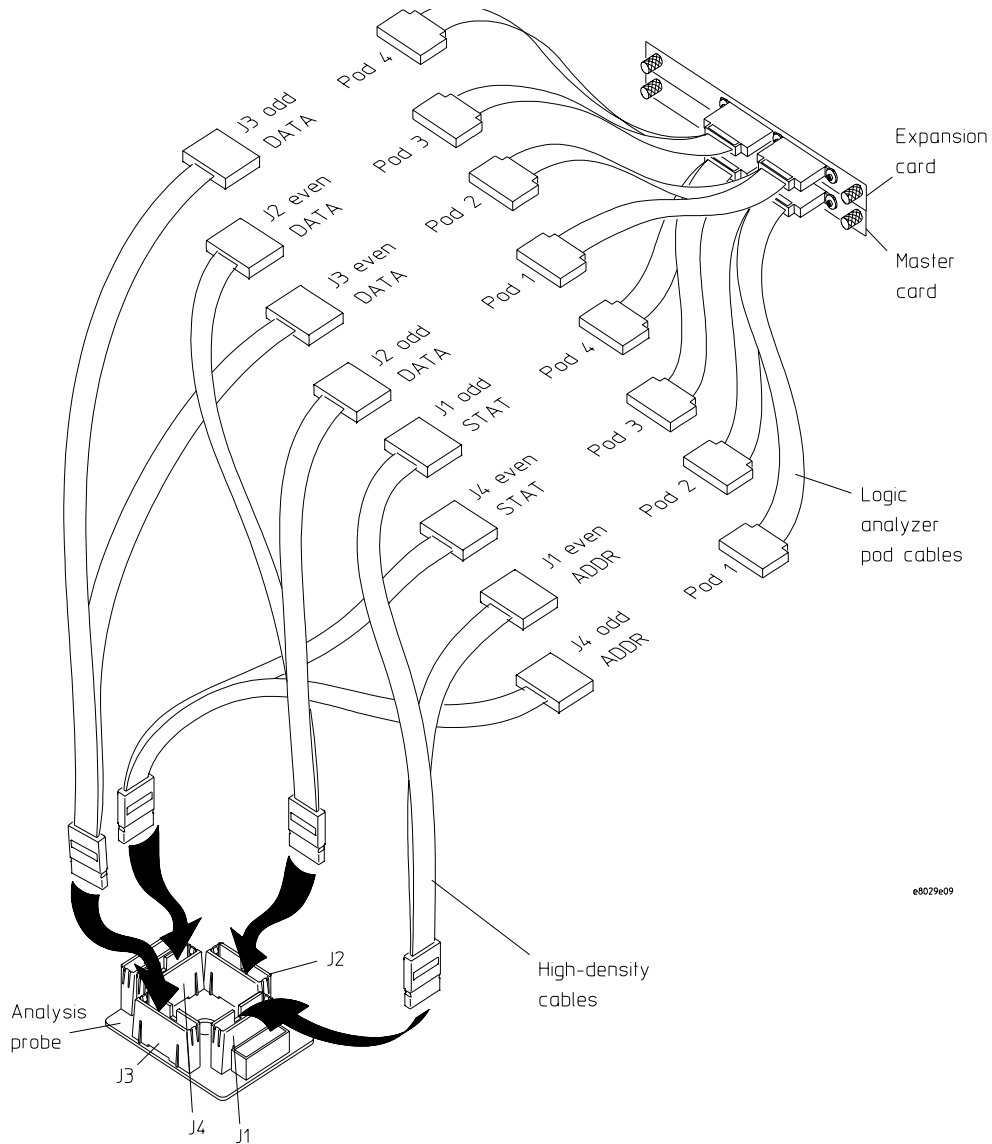
Connect the pod cables to the Analysis Probe according to the pod diagram below.



e8029e17

## Connection Type 'D' To connect to the 16555/56/57A two-cards analyzer

Connect the pod cables to the Analysis Probe according to the pod diagram below.

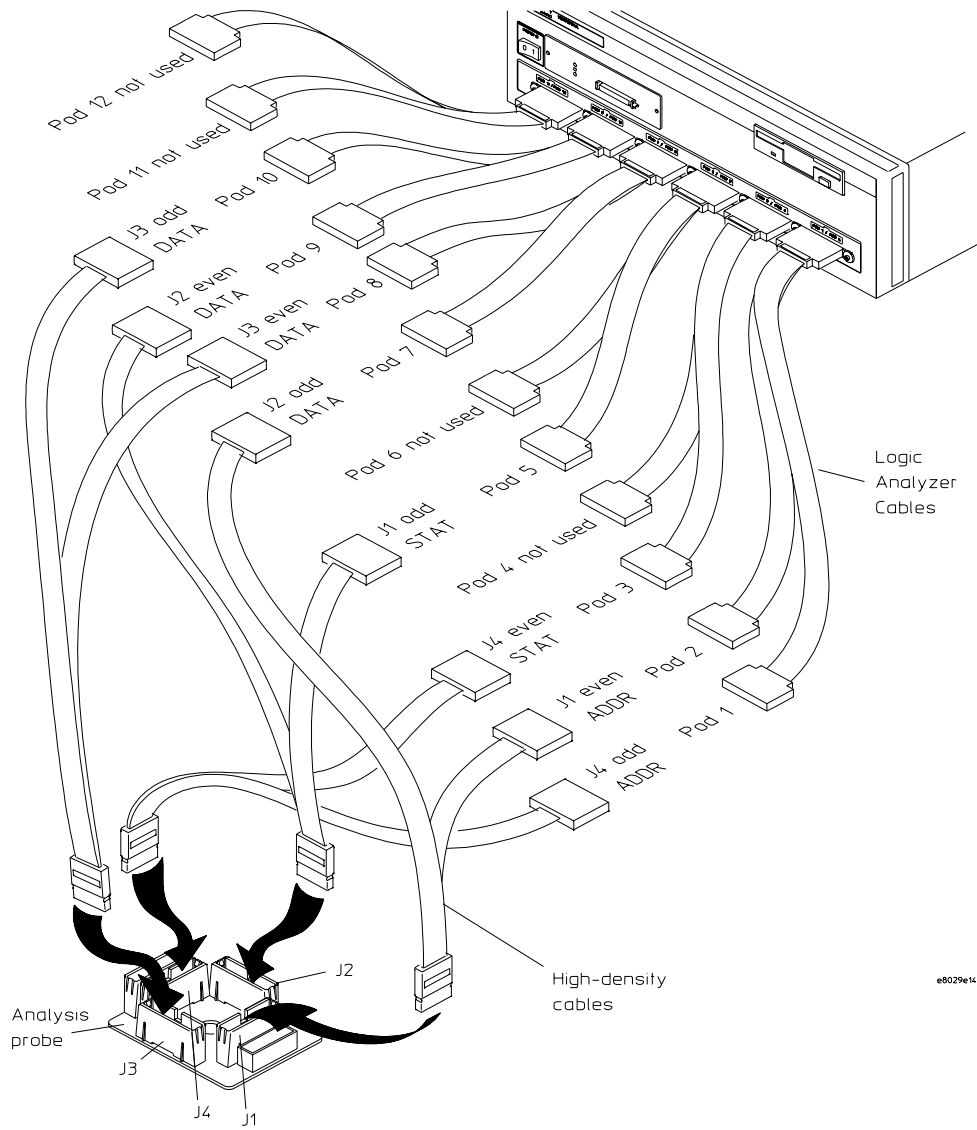


e8029e09



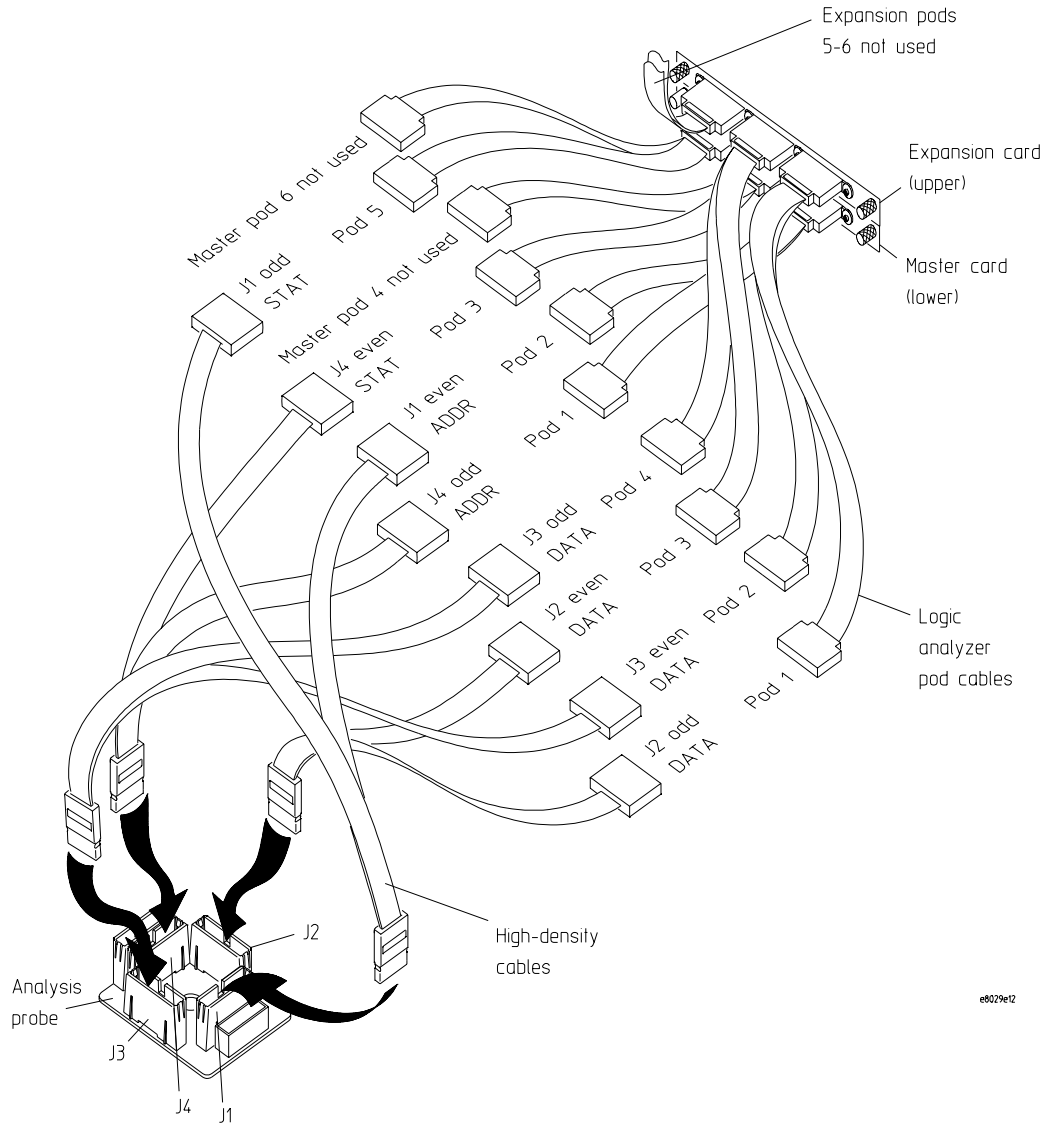
## Connection Type 'E' To connect to the 16600/1A analyzer

Connect the pod cables to the Analysis Probe according to the pod diagram below.



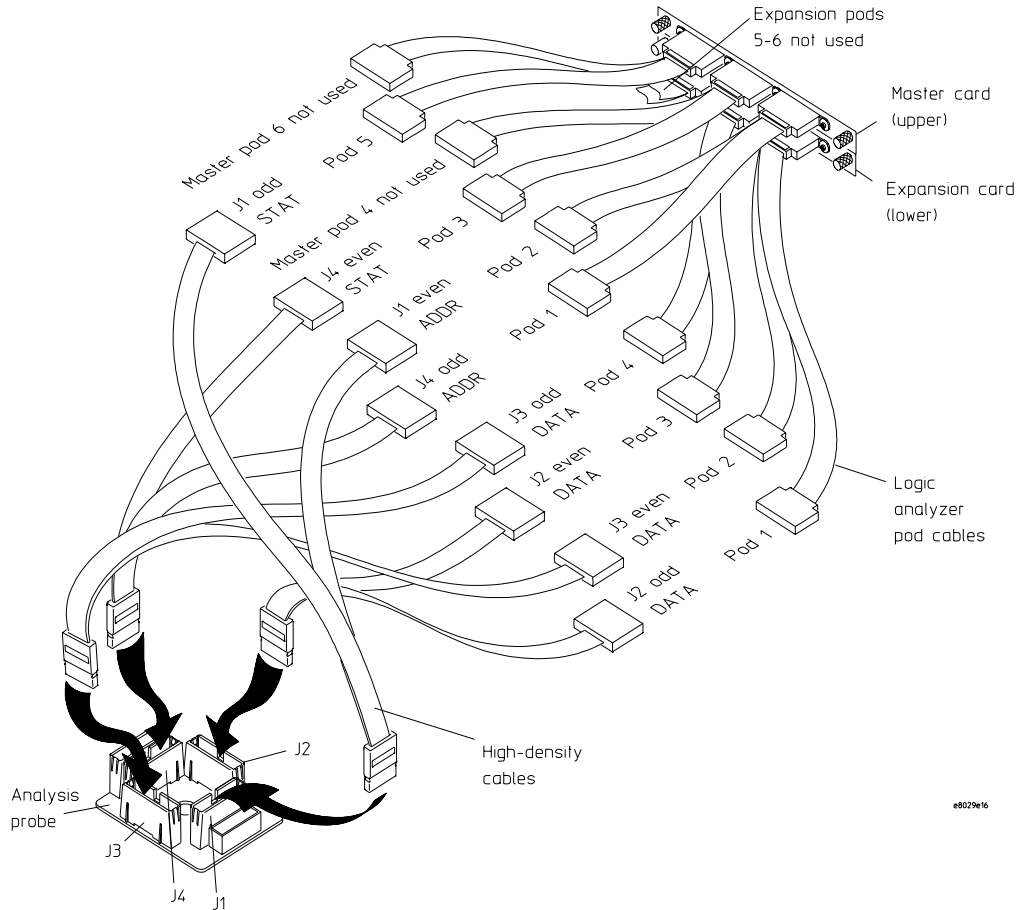
## Connection Type 'F' To connect to the 16550A two-cards analyzer

Connect the pod cables to the Analysis Probe according to the pod diagram below.



## Connection Type 'G' To connect to the 16710/1/2A two-cards analyzer

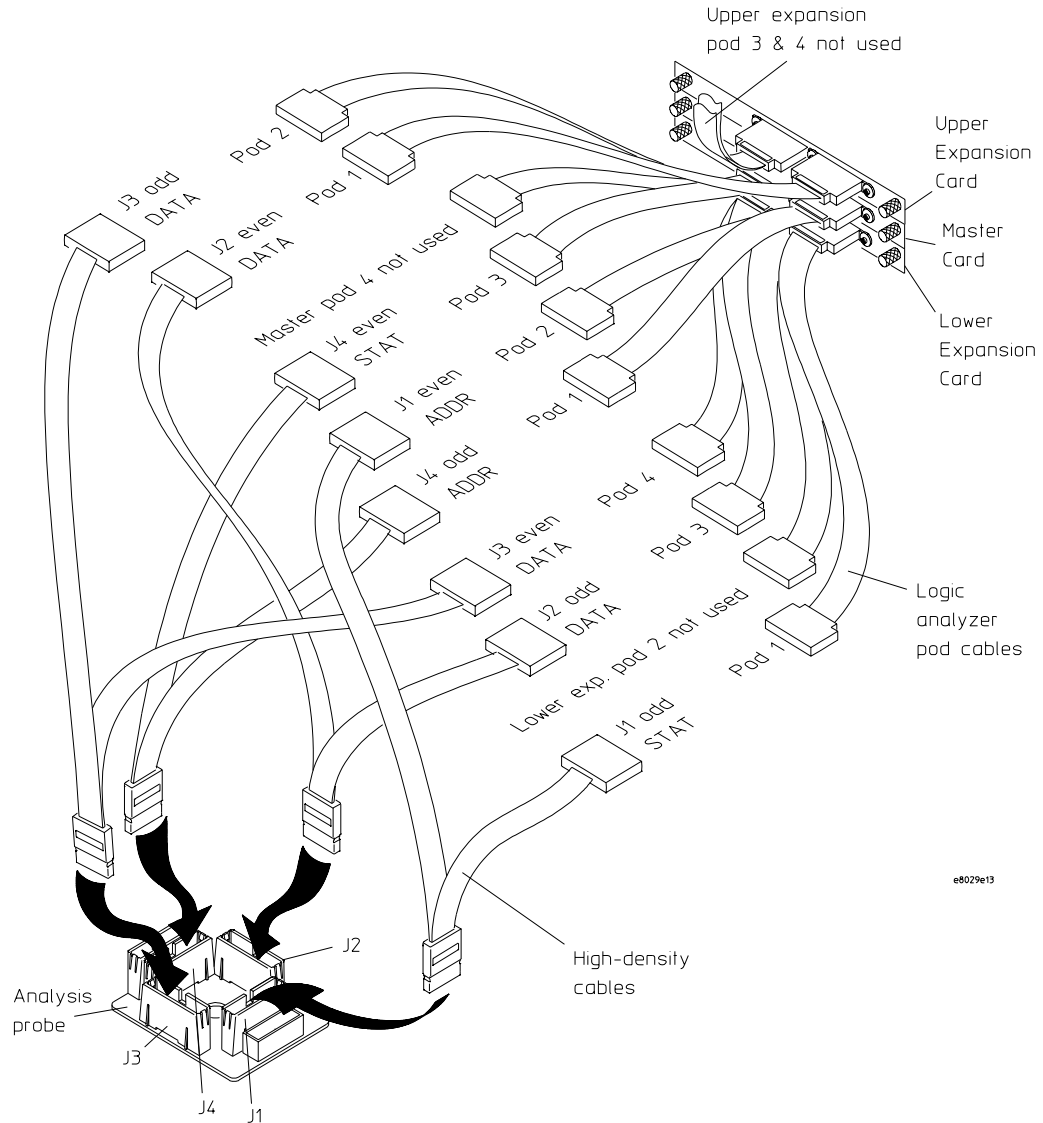
Connect the pod cables to the Analysis Probe according to the pod diagram below.



e8029e16

## Connection Type 'H' To connect to the 16555/56/57A three-cards analyzer

Connect the pod cables to the Analysis Probe according to the pod diagram below.



---

**CAUTION**

All operations must be done on the Agilent Technologies B3759A (Emulation Interface Software) except for the MSA.

After finishing MSA, don't touch anything on the state analysis listing window, although it pops up. Any changing on this window might cause a fatal error on a Agilent Technologies B3759A (Emulation Interface Software).

You can still operate other modules like analog scope. Also as long as you don't remove a state analysis machine, you can operate a workspace to perform cross domain measurement.

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Designing Connectors for  
Custom Probing for the B3759A  
#710 software

---

## Designing Connectors for Custom Probing for the B3759A #710 software

This chapter shows you how to design logic analyzer connectors on your target system for use with the Agilent Technologies B3759A #710 emulation solution user interface software.

If you are using an Agilent Technologies E8029A analysis probe, skip this chapter.

This chapter consists of the following sections:

- Using the General Purpose (GP) probes
- Designing logic analyzer connectors on your target system for the Agilent Technologies B3759A #710 emulation solution user interface software.



## Direct Probing with GP Probes

If you are using general-purpose (GP) probes, connect the individual probes to the signals according to the signal-to-connector mapping tables, as shown in chapter 10. Use the figures in chapter 3 to determine which logic analyzer pods to use for the signal groups.

It is helpful to label the probe headers before installing the probes. You should connect the ground signal for the analyzer clock(s), and two to four signal grounds per pod.

## Designing and Using Built-in Connectors

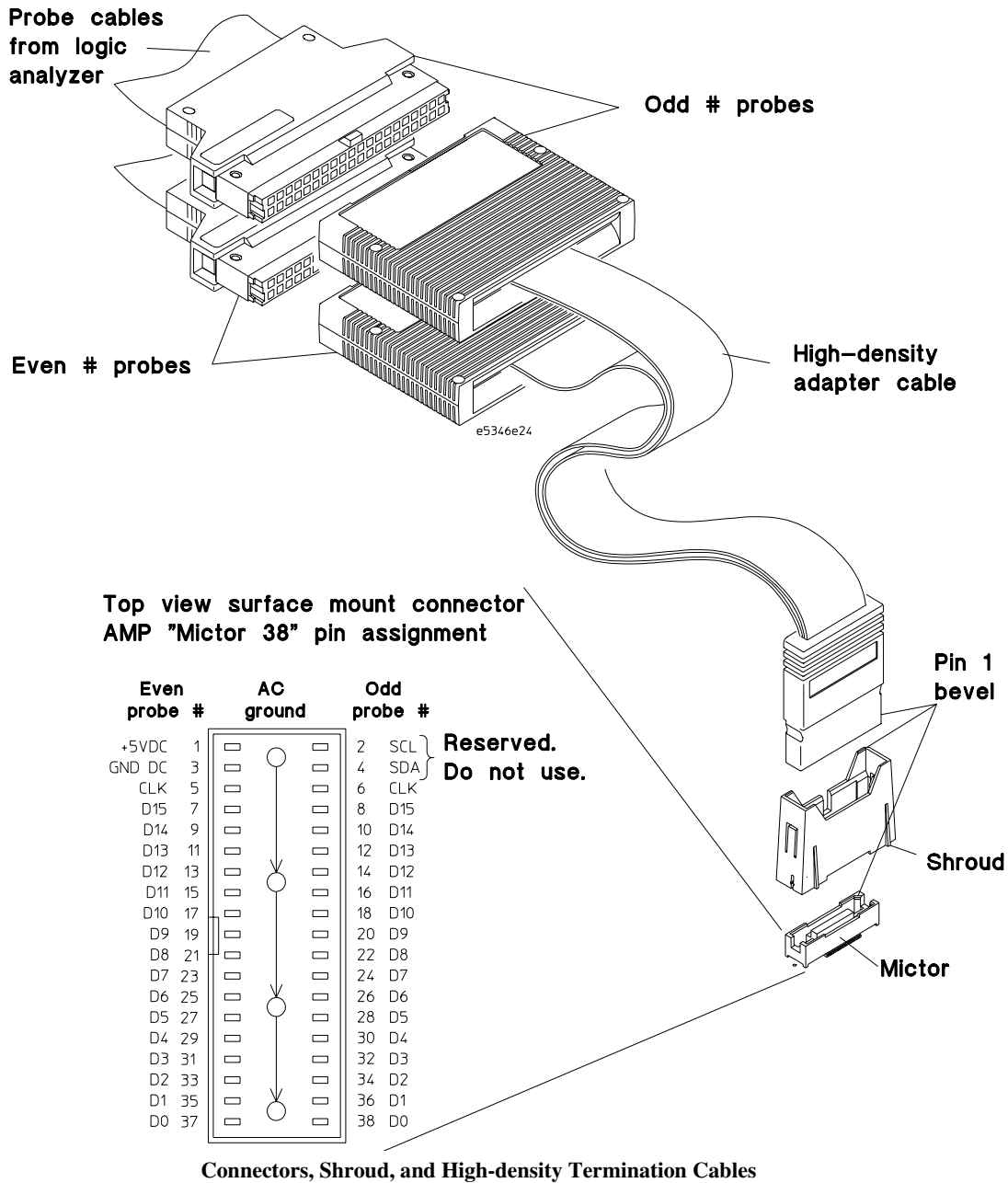
You can design analyzer-compatible connectors into the target board, and connect the logic analyzer cables to these connectors according to the figures in chapter 3. The primary concerns when using built-in connectors are:

- The board real estate required by the connectors
- Ensuring that the logic analyzer connection is properly terminated
- Ensuring that the microprocessor pins connect to the proper logic analyzer probes. See the "Hardware Reference" chapter for pinouts.

The connection scheme shown in this section uses 38-pin connectors on the target system, and high-density termination cables to connect to the logic analyzer. Each connector and cable supports two logic analyzer pods. The part numbers for built-in connectors and cables are shown below. An illustration of the components is shown on the following page.

### Part Numbers for Built-in Connectors and Cables

Part Number	Description
Agilent 1252-7431, or AMP 2-767004-2	2 x 19 header. A minimum of three connectors (six logic analyzer pods) is required; up to six may be used.
Agilent E5346-44701	Optional connector-support shroud
Agilent E5346A	High-density termination cable. One required for each 2x19 connector.



## AMP Mictor 38 Connectors

Each Mictor 38 connector carries 32 signals plus two clocks (CLK1 for two logic analyzer pods). The high-density termination cables are required to connect the logic analyzer cables to the connector (Agilent part number E5346A). These cables contain the required termination. One cable is required for every two logic analyzer pods.

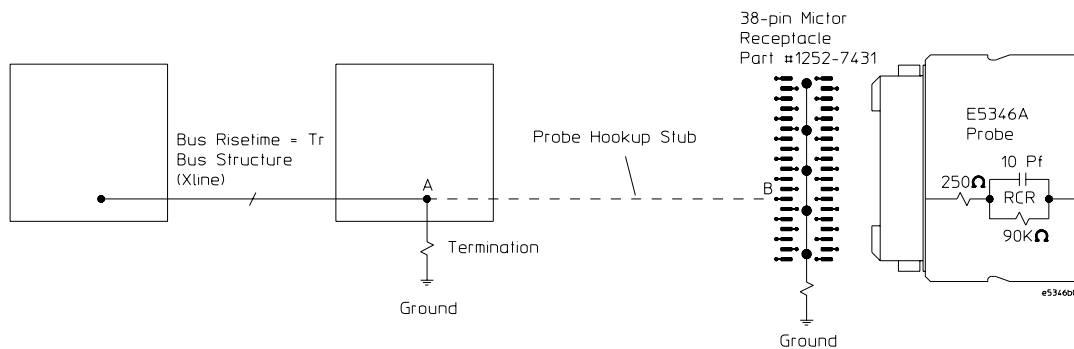
The figure on the previous page shows the pinout for a Mictor 38 connector. Refer to the "Hardware Reference" chapter (page <Reference>) for the tables showing the microprocessor signals for each pin. Note that the +5V pin (pin 1) is used to supply power from the logic analyzer to any active devices on an interface board. In most instances, this pin should not be used.

To increase the structural support for the cables, you can also use cable support shrouds (Agilent part number E5346-44701) on each connector. The figures on the following page show the mechanical layouts for the shrouds and headers.

### Design Considerations

The connector must be located close enough to the target signal so that the stub length created is less than  $\frac{1}{5}$  the  $T_r$  (bus risetime, see figure below). For PC board material, ( $\epsilon_r = 4.9$ ) and  $Z_0$  in the range of 50 - 80 $\Omega$ , use a propagation delay of 160 ps/inch of stub.

Each probed signal line must be able to supply a minimum of 600 mV to the probe tip and handle a minimum of 90 K $\Omega$  shunted by 10 pF. The maximum input voltage to the high-density cables is  $\pm 40$ V peak.

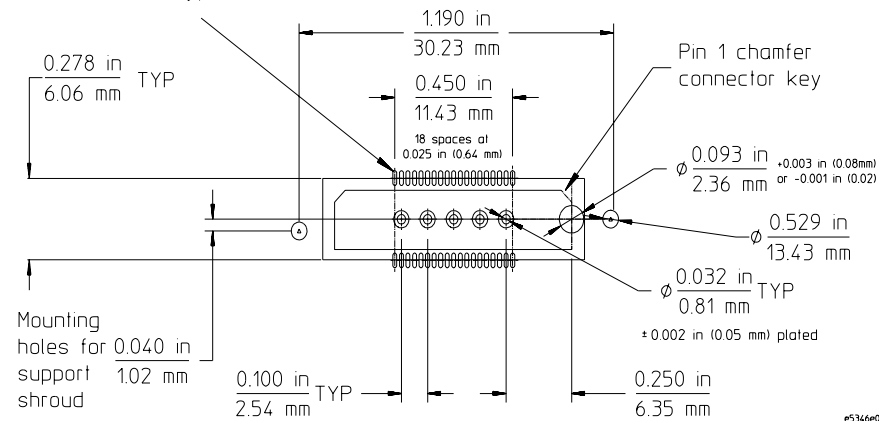


### 2x19 Header Design Rules

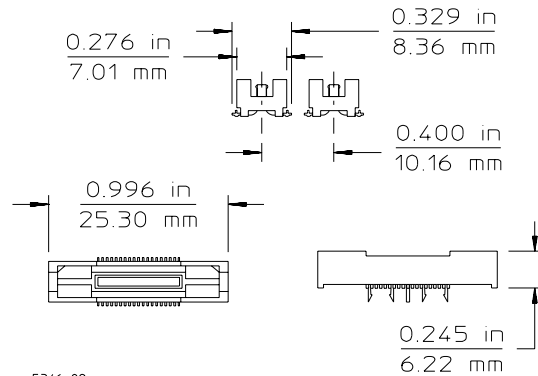
## Support shroud

The support shrouds (Agilent part number E5346-44701) provides additional strain relief between the connectors and the high-density termination cables. The shroud requires two through-hole connections to the target board. It fits around the header, and mounts directly to the target board. The following figures show the mechanical connections for the shrouds and connectors.

0.050 in X 0.017 in (1.27 mm X 0.43 mm)  
 pad with 0.005 in (0.13 mm) X 45°  
 corner chamfers typ 38

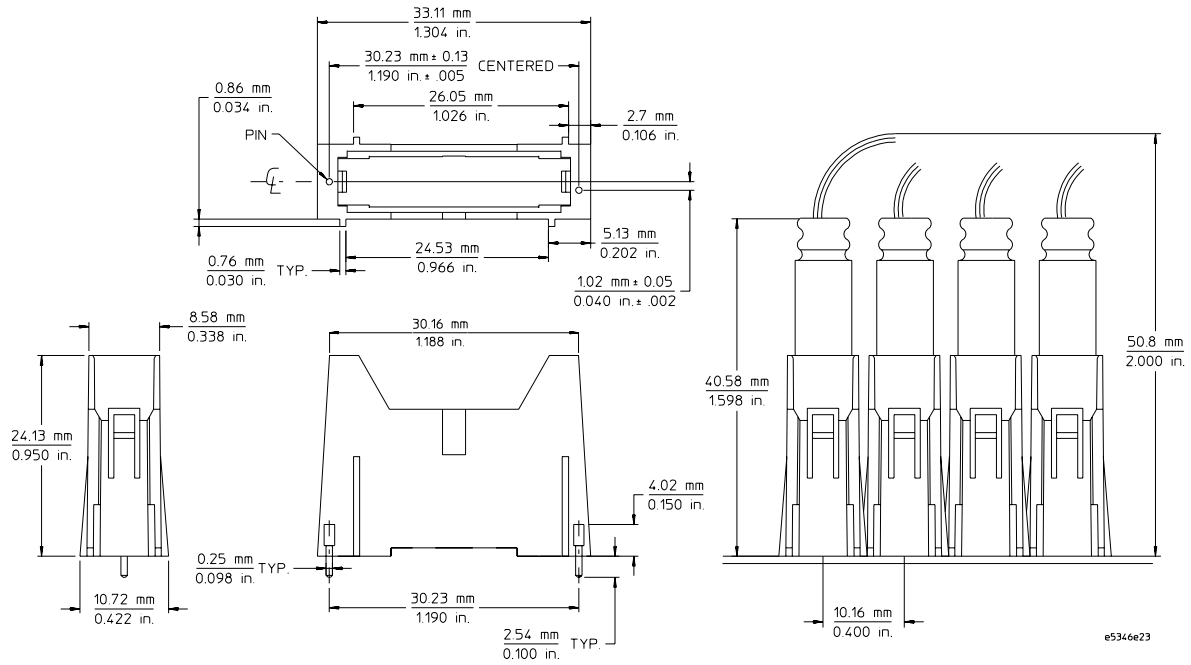


e5346e08



e5346e09

### Support Shroud Mechanical Information



**2x19 Header Mechanical Information**

## Connecting the Logic Analyzer to the Target System Connectors

The procedures for connecting and configuring the logic analyzer are listed in chapter 3.





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## Installing the Emulation Module

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## Installing the Emulation Module

This chapter shows you how to install an emulation module in your Agilent Technologies 16600A/700A-series logic analysis system.

If your emulation module is already installed in your logic analysis system frame, you may skip this chapter.

---

**CAUTION**

These instructions are for trained service personnel. To avoid dangerous electric shock, do not perform any service unless qualified to do so. Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Electrostatic discharge can damage electronic components. Use grounded wriststraps and mats when you handle modules.

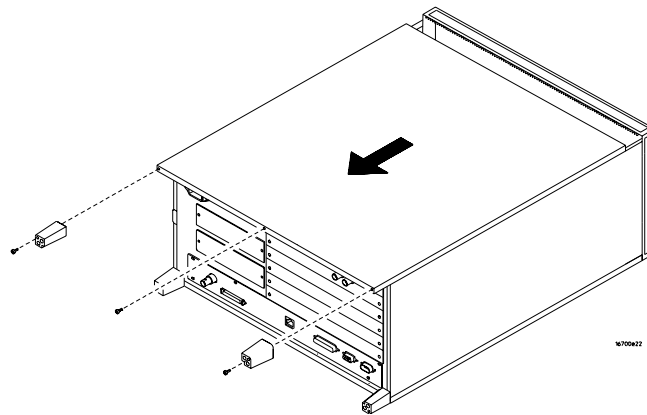
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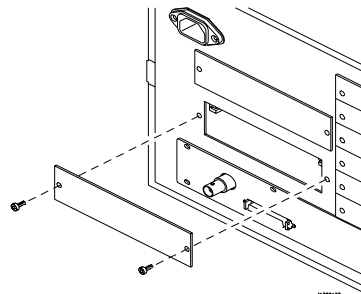
To install the emulation module in a 16700A-series logic analysis system or a 16701A expansion frame

You will need T-10 and T-15 Torx screw drivers.

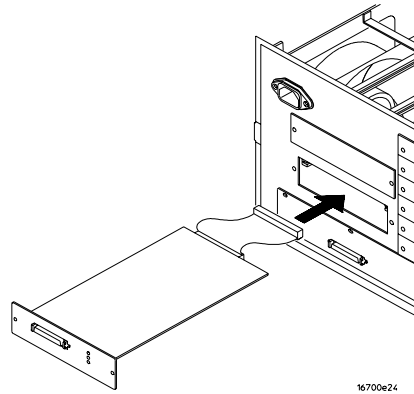
- 1 Turn off the logic analysis system and **REMOVE THE POWER CORD**. Remove any other cables (such as probes, mouse, or video monitor).
- 2 Turn the logic analysis system frame upside-down.
- 3 Remove the bottom cover.



- 4 Remove the slot cover.  
You may use either slot.

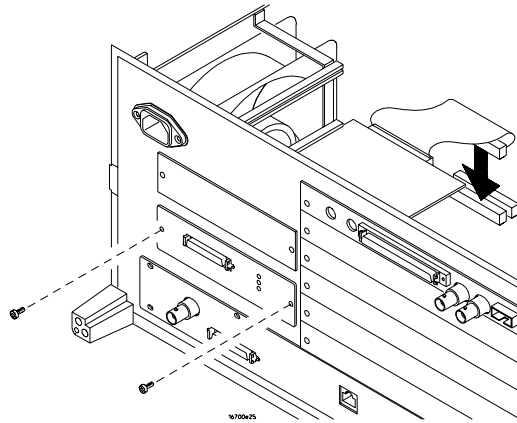


**5** Install the emulation module.



**6** Connect the cable and re-install the screws.

You may connect the cable to either of the two connectors. If you have two emulation modules, note that many debuggers will work only with the "first" module: the one toward the top of the frame ("Slot 1"), plugged into the connector nearest the back of the frame.



**7** Reinstall the bottom cover, then turn the frame right-side-up.

**8** Plug in the power cord, reconnect the other cables, and turn on the logic analysis system.

The new emulation module will be shown in the system window.

**See Also**

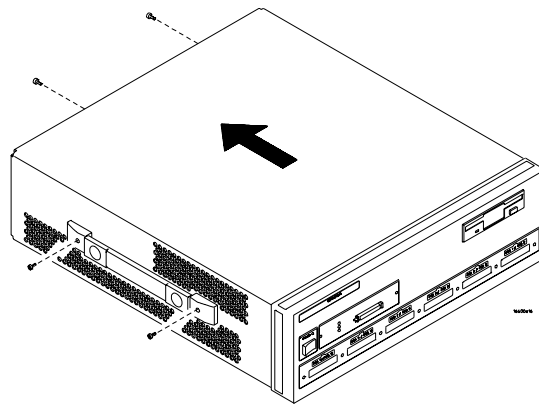
See page 15 for information on giving the emulation module a "personality" for your target processor.

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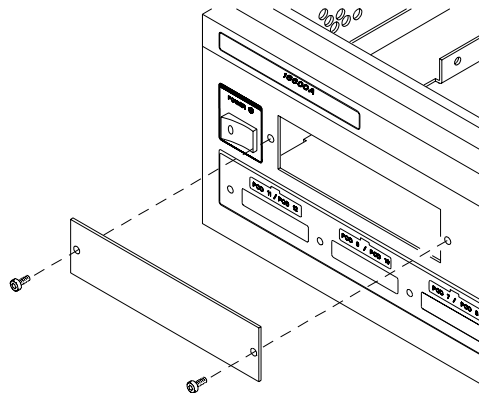
To install the emulation module in a 16600A-series logic analysis system

You will need T-8, T-10, and T-15 Torx screw drivers.

- 1 Turn off the logic analysis system and **REMOVE THE POWER CORD**. Remove any other cables (such as probes, mouse, or video monitor).
- 2 Slide the cover back.

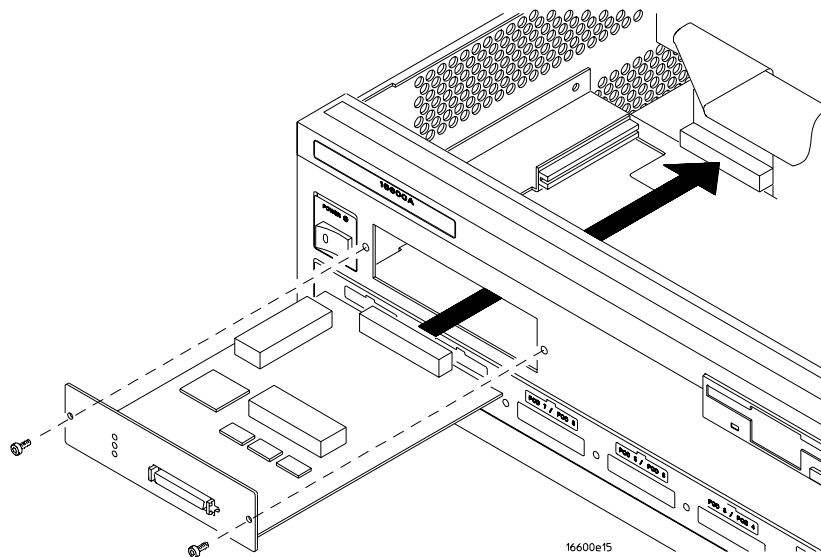


- 3 Remove the slot cover.



Chapter 5: Installing the Emulation Module  
**Installing the Emulation Module**

- 4 Install the emulation module.
- 5 Connect the cable and re-install the screws.



- 6 Reinstall the cover.  
Tighten the screws snugly ( 2 N•m or 18 inch-pounds).
- 7 Plug in the power cord, reconnect the other cables, and turn on the logic analysis system.  
The new emulation module will be shown in the system window.

**See Also**

See page 15 for information on giving the emulation module a "personality" for your target processor.

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## Connecting the Emulator

---

# Connecting the Emulator

This chapter shows you how to connect the emulator to the target system and how to configure the emulator and target processor.

## Overview

Here is a summary of the steps for connecting and configuring the emulator:

- 1 Make sure the target system is designed to work properly with the emulator. (Page 68.)
- 2 Install the emulation module in your logic analysis system, if necessary. (Page 57.)  
If you are connecting an emulation module to an Agilent Technologies 16600A/700A-series logic analysis system, use the Setup Assistant to guide you through steps 3-4.
- 3 Connect the emulator to your target system using the 50-pin cable and the TIM or an analysis probe. (Page 71.)
- 4 Update the firmware of the emulator, if necessary. (Page 15.)
- 5 Verify communication between the emulator and the target.
- 6 Configure the emulator
- 7 Test the connection between the emulator and the target.
- 8 Connect a debugger to the emulator, if applicable.



## Using the Emulation Control Interface

The Emulation Control Interface in your Agilent Technologies 16600A/700A-Series logic analysis system allows you to control an emulator (an emulation module or an emulation probe).

As you set up the emulator, you will use the Emulation Control Interface to:

- Update firmware (which preloads or changes the processor-specific personality of the emulator).
- Change the LAN port assignment (rarely necessary).
- Run performance verification tests on the emulator.

The Emulation Control Interface allows you to:

- Run, break, reset, and step the target processor.
- Set and clear breakpoints.
- Read and write registers.
- Read and write memory.
- Read and write I/O memory.
- View memory in mnemonic form.
- Read and write the emulator configuration.
- Download programs (in Motorola S-Record or Intel Hex format) to the target system RAM or ROM.
- View emulator status and errors.
- Write and play back emulator command script files.

If you have an emulation probe, this interface also allows you to configure the LAN address of the emulation probe.

Using the logic analysis system's intermodule bus does not require the Emulation Control Interface to be running. If the emulation module icon is in the Intermodule window, then it will be able to send and receive signals. Therefore if you are using a debugger, you can use an analyzer to cause a break.

Using a debugger with the Emulation Control Interface is not recommended because:

- The interface can get out of synchronization when commands are issued from both interfaces. This causes windows to be out-of-date and can cause confusion.
- Most debuggers cannot tolerate another interface issuing commands and may not start properly if another interface is running.

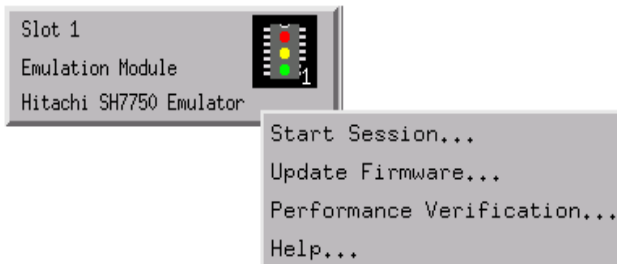
**See Also**

All of the Emulation Control Interface windows provide online help with a Help button or a Help->On this window menu selection. Refer to the online help for complete details about how to use a particular window.

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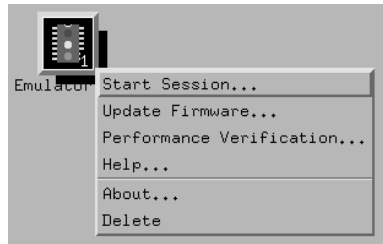
### To start the Emulation Control Interface from the main System window (emulation module)

- 1 In the System window, click the emulation module icon.
- 2 Select **Start Session...**



### To start the Emulation Control Interface from the Workspace window (emulation module)

- 1 Open the Workspace window.
- 2 Drag the Emulator icon onto the workspace.
- 3 Right-click the Emulator icon, and then select **Start Session...**

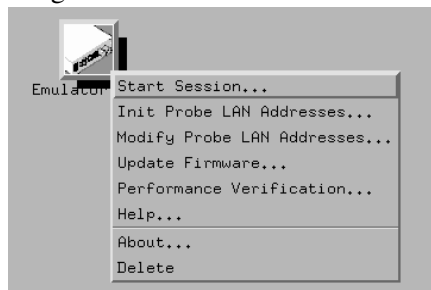


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### To start the Emulation Control Interface from the Workspace window (emulation probe)

If you have a stand-alone emulation probe connected to the logic analysis system via LAN, use the Emulation Probe icon instead of the Emulation Module icon.

- 1 Open the Workspace window.
- 2 Drag the Emulation Probe icon onto the workspace.
- 3 Right-click the Emulation Probe icon, and select **Start Session...**



- 4 In the Session window, enter the IP address or LAN name of the emulation probe, then click **Start Session**.

## Designing a Target System

This section will help you design a target system that will work with the Agilent Technologies E3467A Emulation Module.

---

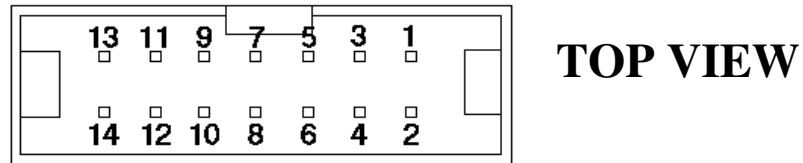
### Wiring the N-wire

To connect the Agilent Technologies E3467A Emulation Module to your target system, you have to prepare the following 14 signals called N-wire on your target system using the 14-pin connector.

#### N-wire

Cable Pin Number	Signal	SH7750 Pin Number	
		QFP	BGA
1	TCK	198	A5
3	/TRST	200	C4
5	TDO	194	A6
7	/ASEBRK	193	B7
9	TMS	197	B6
11	TDI	199	B5
13	/RESET	2	B1
8	V <sub>DD</sub> (3.3V)		
Even Pins (Except for pin 8)	V <sub>SS</sub>		

Pin assignments for 14-pin connector is the following.



### 14-pin connector

You can use following connectors.

Supplier	Product Number	Description
Sumitomo3M (Japan)	7614-6002	Low profile straight header connector
3M (U.S.A)	2514-6002UB	Low profile straight header connector

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#### CAUTION

Locate the 14-pin connector within 10cm (4 inches) from the microprocessor on your target system. If the 14-pin connector is located further than 10cm (4 inches) away from the microprocessor, Agilent Technologies E3467A Emulation Probe may not work correctly.

---

### Target $V_{DD}$

The Agilent Technologies E3467A Emulation Module may draw up to 10 mA from target  $V_{DD}$ .

## Precautions when you design your target system

You need to pay attention to the following limitations when you design your target system.

### **/TRST signal**

You must design your target board so /TRST is driven to low during RESET upon the target power-on. It should be designed so the emulation probe is also able to control the signal by itself.

## Connecting the Emulator to the Target System

Choose one of the following methods for connecting the emulator to a target system.

- Directly through a debug port connector on the target board.
- Through an Agilent Technologies E9598A analysis probe, which provides a direct connection to the debug port pins.

After you have connected the emulator to your target system, you may need to update the firmware in the emulator.

**See Also**

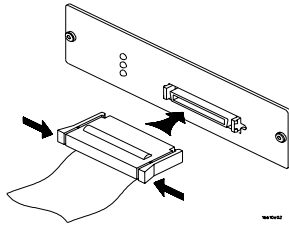
For information on designing a debug port on your target board, see page 68.

For a list of the parts supplied with the emulator, see page 21.

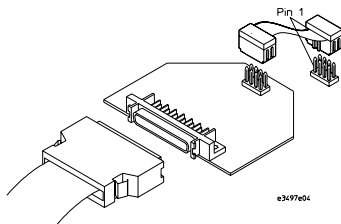
## To connect to a target system using a debug port

The emulator can be connected to a target system through a 7-pin debug port. The emulator should be connected to a 14-pin male 2x5 header connector on the target system using the 14-conductor cable assembly provided.

- 1 Turn off the target system and disconnect it from all power sources.
- 2 Plug one end of the 50-pin cable into the emulator.



- 3 Plug one end of the 14-pin cable into the target interface module.
- 4 Plug the other end of the 14-pin cable into the debug port on the target system.



- 5 Turn on the power to the logic analysis system and **then the target system.**

### See Also

"Designing a Target System" (page 68) for information on designing a target system for use with the emulator.



### To connect to a target system using an analysis probe

- 1 Remove power from the target system.
- 2 Plug one end of the 50-pin cable into the emulator.
- 3 Plug the other end of the 50-pin cable into the connector on the analysis probe.

## To update Firmware

Always update firmware by installing a processor support package. This will ensure that the version of the Emulation Control Interface software is compatible the version of the emulator firmware.

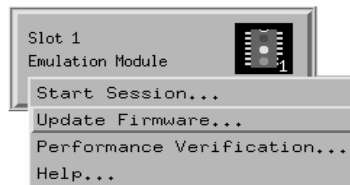
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### To display current firmware version information

- 1 In the Update Firmware window, click Display Current Version.  
There are usually two firmware version numbers: one for “Generics” and one for the personality of your processor.
- 

### To update firmware for an emulation module using the Emulation Control Interface

- 1 End any run control sessions which may be running.
- 2 In the Workspace window, remove any Emulator icons from the workspace.
- 3 Install the processor support package from the CD-ROM, if necessary.
- 4 In the system window, click the emulation module and select **Update Firmware...**



- 5 In the Update Firmware window, select the firmware to load into the emulation module.
- 6 Click **Update Firmware**.  
In about 20 seconds, the firmware will be installed and the screen will update to show the current firmware version.

#### See Also

“Installing Software” beginning on page 38 for instructions on how to install the processor support package from the CD-ROM.

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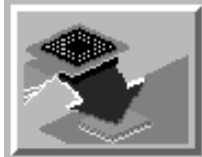
## To update firmware for an emulation module using the Setup Assistant

The Setup Assistant is an online tool for connecting and configuring your logic analysis system for microprocessor and bus analysis. The Setup Assistant is available on the Agilent Technologies 16600A and 16700A-series logic analysis systems.

This menu-driven tool will guide you through the connection procedures for connecting the logic analyzer to an analysis probe, an emulation module, or other supported equipment. It will also guide you through connecting an analysis probe to the target system.

Do not use the Setup Assistant to connect an emulation probe if you already have an emulation module installed.

- 1 Install the processor support package from the CD-ROM.
- 2 Start the Setup Assistant by clicking its icon in the system window.



- 3 Follow the instructions displayed by the Setup Assistant.

### See Also

Page 51 for instructions on how to install a the processor support package from the CD-ROM.

## Configuring the Emulator

The emulator has several user-configurable options. These options may be customized for specific target systems and saved in configuration files for future use.

The easiest way to configure the emulator is through the Emulation Control Interface in an Agilent Technologies 16600A or 16700A logic analysis system.

If you use the Emulation Control Interface, please refer to the online help in the Configuration window for information on each of the configuration options.

You may also use the emulator configuration window of your debugger (B3759A #710) to configure your emulator.

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## To configure using the Emulation Control Interface

The easiest way to configure the emulators is to use the Emulation Control Interface.

### 1 Start an Emulation Control Interface session.

From an emulation module:

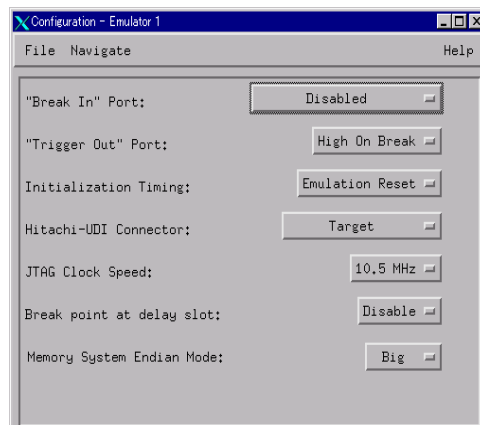
- In the system window, click the Emulation Control Interface icon, and then select “Start Session...”.

For an emulation probe:

- In the workspace window, drag the emulation probe icon onto the workspace, and then select “Start Session...”.

### 2 Open a Configuration window.

Select “Configuration...” from the Emulation Control Interface icon or from the Navigate menu in any Emulation Control Interface window.



### 3 Set the configuration options, as needed.

The configuration selections will take effect when you close the configuration window or when you move the mouse pointer outside the window.

### 4 Save the configuration settings.

To save the configuration settings, open the File Manager window and click **Save....**

#### See Also

Help->**Help on this window** in the Configuration window for information on each of the configuration options.

Help in the Emulation Control Interface menu for help on starting an Emulation Control session.

## Testing the emulator and target system

After you have connected and configured the emulator, you should perform some simple tests to verify that everything is working.

**See Also**

“Troubleshooting the Emulator” on page 107 for information on testing the emulator hardware.

---

### To test memory accesses

- 1 Start the Emulation Control Interface and configure the emulator, if necessary.
  - 2 Open the Memory window.
  - 3 Write individual locations or fill blocks of memory with patterns of your choosing.  
The access size is the size of memory access that will be used to write or read the memory values.
  - 4 Use the Memory I/O window to stimulate I/O locations by reading and writing individual memory locations.
- 

### To test with a running program

To more fully test your target, you can load simple programs and execute them.

- 1 Compile or assemble a small program and store it in a Motorola S-Record or Intel Hex file.
  - 2 Use the Load Executable window to download the program into RAM or flash memory.
  - 3 Use the Breakpoints window to set breakpoints. Use the Registers window to initialize register values.  
The new register or breakpoint values are sent to the processor when you press the Enter key or when you move the cursor out of the selected register field.
  - 4 In the Run Control window, click Run.
  - 5 Use the Memory Mnemonic window to view the program and use the Memory window to view any output which has been written to memory.
-

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Hardware Reference

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## Hardware Reference

This chapter contains additional reference information including the specifications and characteristics for the analysis probe and the emulation probe, as well as signal mapping for the Agilent Technologies E8029A analysis probe and the B3759A #710 software. It consists of the following information:

- Analysis probe reference
- Emulation module reference



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## Analysis probe-operating characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the Agilent Technologies E8029A SH7750 analysis probe.

### Product Characteristics

Microcontroller Supported	Hitachi SH7750
Package Supported	208-pin QFP
Pods Required	8, or 10 logic analyzer pods (four high-density adapter cables) are required for disassembly depending on your target system's memory. Two high-density adapter cables are available for additional signal analysis.

### Electrical Characteristics

Power Requirements	None.
Signal Line Loading	10pF, 100 kohms on all signals.

### Environmental Characteristics

Temperature	Operating	0 to + 50 degrees C +32 to +131 degrees F
Altitude	Operating	4,600 m 15,000 feet
Humidity		Up to 75% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation on the circuit board.

---

## Theory of operation

The Agilent Technologies E8029A analysis probe is a passive probe. All signals are routed through to the logic analyzer without passing through any additional circuitry.

---

## Analysis probe - signal-to-connector mapping

The following tables show the electrical signal-to-connector mapping implemented by the Agilent Technologies E8029A SH7750 Analysis Probe and the B3759A #710 interface software.

**SH7750 Signal List**

Connector	Analyzer Bit	SH7750 Pin #	Signal Name	Analyzer Label	Analyzer Label
J1odd (6)	CLK1	165	TCLK		
J1odd (8)	15	8	BS		
J1odd (10)	14	7	CS6		
J1odd (12)	13	6	CS5		
J1odd (14)	12	5	CS4		
J1odd (16)	11	89	CS3		
J1odd (18)	10	90	CS2		
J1odd (20)	9	4	CS1		
J1odd (22)	8	3	CS0		
J1odd (24)	7	1	RDY		
J1odd (26)	6	192	MD6/IOIS16		
J1odd (28)	5	191	STATUS1		
J1odd (30)	4	190	STATUS0		
J1odd (32)	3	183	MD5/RAS2		
J1odd (34)	2	182	MD4/CE2B		
J1odd (36)	1	181	MD3/CE2A		
J1odd (38)	0	106	DREQ0		
J1even (5)	CLK1	156	NMI		
J1even (7)	15	155	IRL3		
J1even (9)	14	154	IRL2		
J1even (11)	13	153	IRL1		
J1even (13)	12	152	IRL0		
J1even (15)	11	185	DACK1		
J1even (17)	10	184	DACK0		
J1even (19)	9	180	A25		
J1even (21)	8	179	A24		
J1even (23)	7	176	A23		
J1even (25)	6	175	A22		
J1even (27)	5	174	A21		
J1even (29)	4	173	A20		
J1even (31)	3	172	A19		
J1even (33)	2	171	A18		
J1even (35)	1	62	A17		
J1even (37)	0	63	A16		

Connector	Analyzer Bit	SH7750 Pin #	Signal Name	Analyzer Label	Analyzer Label
J2odd (6)	CLK1	2	RESET		
J2odd (8)	15	33	D15		
J2odd (10)	14	35	D14		
J2odd (12)	13	37	D13		
J2odd (14)	12	41	D12		
J2odd (16)	11	45	D11		
J2odd (18)	10	47	D10		
J2odd (20)	9	49	D9		
J2odd (22)	8	53	D8		
J2odd (24)	7	54	D7		
J2odd (26)	6	50	D6		
J2odd (28)	5	48	D5		
J2odd (30)	4	46	D4		
J2odd (32)	3	42	D3		
J2odd (34)	2	38	D2		
J2odd (36)	1	36	D1		
J2odd (38)	0	34	D0		
J2even (5)	CLK1	208	SCK2/MRESET		
J2even (7)	15	11	D47		
J2even (9)	14	15	D46		
J2even (11)	13	17	D45		
J2even (13)	12	19	D44		
J2even (15)	11	23	D43		
J2even (17)	10	25	D42		
J2even (19)	9	27	D41		
J2even (21)	8	29	D40		
J2even (23)	7	30	D39		
J2even (25)	6	28	D38		
J2even (27)	5	26	D37		
J2even (29)	4	24	D36		
J2even (31)	3	20	D35		
J2even (33)	2	18	D34		
J2even (35)	1	16	D33		
J2even (37)	0	12	D32		

Chapter 7: Hardware Reference  
**Analysis probe - signal-to-connector mapping**

Connector	Analyzer Bit	SH7750 Pin #	Signal Name	Analyzer Label	Analyzer Label
J3odd (6)	CLK1	193	ASEBRKK/BRKACK		
J3odd (8)	15	146	D63		
J3odd (10)	14	142	D62		
J3odd (12)	13	140	D61		
J3odd (14)	12	138	D60		
J3odd (16)	11	134	D59		
J3odd (18)	10	132	D58		
J3odd (20)	9	130	D57		
J3odd (22)	8	128	D56		
J3odd (24)	7	127	D55		
J3odd (26)	6	129	D54		
J3odd (28)	5	131	D53		
J3odd (30)	4	133	D52		
J3odd (32)	3	137	D51		
J3odd (34)	2	139	D50		
J3odd (36)	1	141	D49		
J3odd (38)	0	145	D48		
J3even (5)	CLK1				
J3even (7)	15	124	D31		
J3even (9)	14	122	D30		
J3even (11)	13	120	D29		
J3even (13)	12	116	D28		
J3even (15)	11	112	D27		
J3even (17)	10	110	D26		
J3even (19)	9	108	D25		
J3even (21)	8	103	D24		
J3even (23)	7	102	D23		
J3even (25)	6	104	D22		
J3even (27)	5	109	D21		
J3even (29)	4	111	D20		
J3even (31)	3	115	D19		
J3even (33)	2	119	D18		
J3even (35)	1	121	D17		
J3even (37)	0	123	D16		

Connector	Analyzer Bit	SH7750 Pin #	Signal Name	Analyzer Label	Analyzer Label
J4odd (6)	CLK1	77	CKIO		
J4odd (8)	15	64	A15		
J4odd (10)	14	67	A14		
J4odd (12)	13	68	A13		
J4odd (14)	12	71	A12		
J4odd (16)	11	72	A11		
J4odd (18)	10	73	A10		
J4odd (20)	9	74	A9		
J4odd (22)	8	75	A8		
J4odd (24)	7	76	A7		
J4odd (26)	6	80	A6		
J4odd (28)	5	81	A5		
J4odd (30)	4	82	A4		
J4odd (32)	3	83	A3		
J4odd (34)	2	84	A2		
J4odd (36)	1	189	A1		
J4odd (38)	0	186	A0		
J4even (5)	CLK1	55	CKE		
J4even (7)	15	51	BACK/BSREQ		
J4even (9)	14	52	BREQ/BSACK		
J4even (11)	13	101	WE7/CAS7/DQM7/REG		
J4even (13)	12	98	WE6/CAS6/DQM6		
J4even (15)	11	58	WE5/CAS5/DQM5		
J4even (17)	10	59	WE4/CAS4/DQM4		
J4even (19)	9	97	WE3/CAS3/DQM3/ICIOWR		
J4even (21)	8	96	WE2/CAS2/DQM2/ICIORD		
J4even (23)	7	60	WE1/CAS1/DQM1		
J4even (25)	6	61	WE0/CAS0/DQM0		
J4even (27)	5	94	RD/CASS/FRAME		
J4even (29)	4	93	RAS		
J4even (31)	3	85	DRAK1		
J4even (33)	2	107	DREQ1		
J4even (35)	1	86	DRAK0		
J4even (37)	0	95	RD/WR		

Chapter 7: Hardware Reference  
**Analysis probe - signal-to-connector mapping**

Connector	Analyzer Bit	SH7750 Pin #	Signal Name	Analyzer Label	Analyzer Label
J5odd (6)	CLK1				
J5odd (8)	15				
J5odd (10)	14				
J5odd (12)	13				
J5odd (14)	12				
J5odd (16)	11				
J5odd (18)	10				
J5odd (20)	9				
J5odd (22)	8				
J5odd (24)	7		RXD		
J5odd (26)	6	105	CTS2		
J5odd (28)	5	164	MD7/TXD		
J5odd (30)	4	167			
J5odd (32)	3	166	MD8/RTS2		
J5odd (34)	2	151	MD2/RXD2		
J5odd (36)	1	150	MD1/TXD2		
J5odd (38)	0	149	MD0/SCK		
J5even (5)	CLK1				
J5even (7)	15				
J5even (9)	14				
J5even (11)	13				
J5even (13)	12				
J5even (15)	11				
J5even (17)	10				
J5even (19)	9				
J5even (21)	8				
J5even (23)	7				
J5even (25)	6				
J5even (27)	5				
J5even (29)	4				
J5even (31)	3				
J5even (33)	2				
J5even (35)	1				
J5even (37)	0				

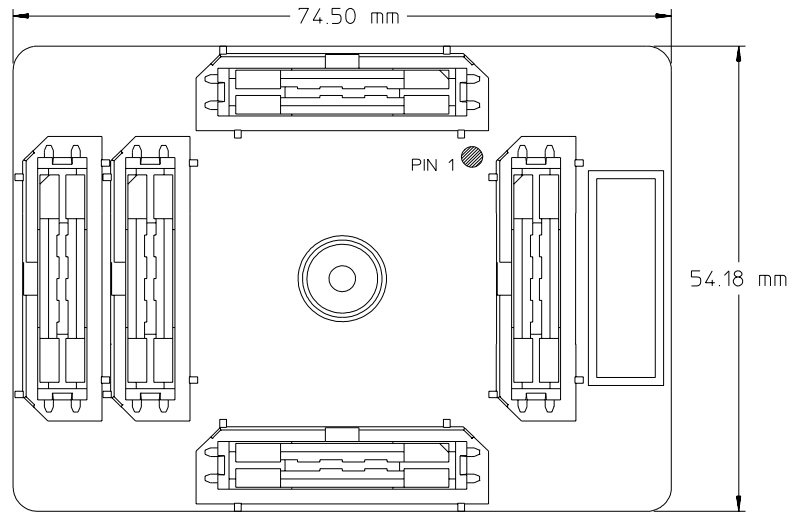
---

**Note** J5 connector is for timing analysis only. You do not need to have this connector if you are performing state analysis only.

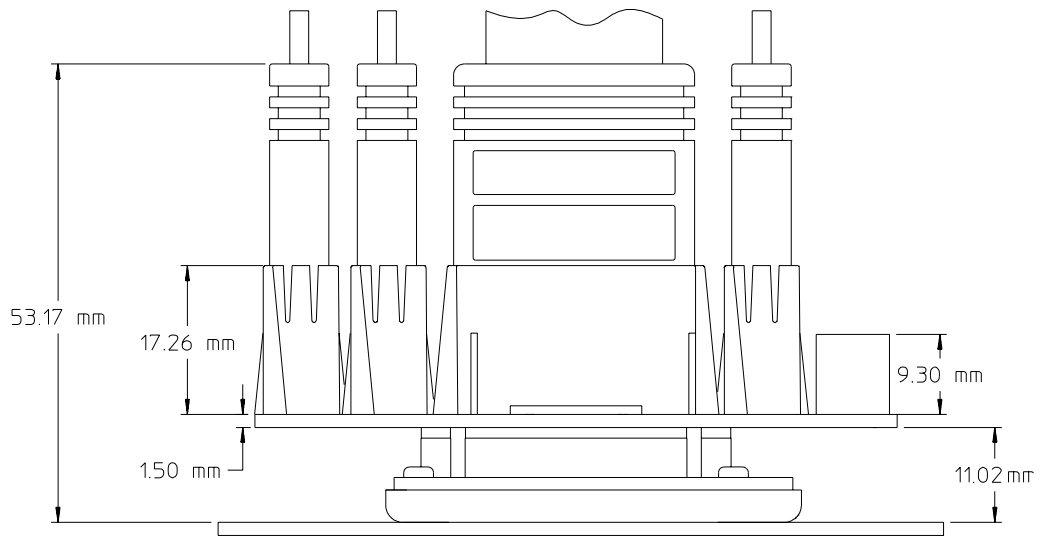
---

## Circuit Board Dimensions

The following figure gives the dimensions for the Analysis Probe assembly. The dimensions are listed in millimeters.



e8029e01



e8029e02

## Emulation module - Operating characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the Agilent Technologies 16610A emulation module and SH7750 target interface module.

---

## Processor Compatibility

The Agilent Technologies E3467A SH7750 emulator supports the SH7750 microprocessor.



---

## Emulation Module Electrical Characteristics

---

### Maximum Ratings

---

Characteristics for the SH7750	Notes	Symbol	Min	Max	Unit
Input voltage range		$V_{in}$	-0.5	5.5	V

## Emulation Module Environmental Characteristics

The Agilent Technologies 16610A emulation module meets the environmental characteristics of the logic analysis system in which it is installed.  
For indoor use only.

---

## Troubleshooting the Analysis Probe

---

## Troubleshooting the Analysis Probe

If you encounter difficulties while making measurements, use this chapter to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions.

If you still have difficulty using the analyzer after trying the suggestions in this chapter, please contact your local Agilent Technologies service center.

### **CAUTION**

When you are working with the analyzer, be sure to power down both the analyzer and the target system before disconnecting or connecting cables, probes, and analysis probes. Otherwise, you may damage circuitry in the analyzer, analysis probe, or target system.

## Logic Analyzer Problems

This section lists general problems that you might encounter while using the logic analyzer.

---

### Intermittent data errors

This problem is usually caused by poor connections, incorrect signal levels, or marginal timing.

- Remove and reseat all cables and probes, ensuring that there are no bent pins on the analysis probe interface or poor probe connections.
- Adjust the threshold level of the data pod to match the logic levels in the system under test.
- Use an oscilloscope to check the signal integrity of the data lines.

Clock signals for the state analyzer must meet particular pulse shape and timing requirements. Data inputs for the analyzer must meet pulse shape and setup and hold time requirements.

**See Also**

See “Capacitive Loading” in this chapter for information on other sources of intermittent data errors.

---

### Unwanted triggers

Unwanted triggers can be caused by instructions that were fetched but not executed.

- Add the prefetch queue or pipeline depth to the trigger address to avoid this problem.

The logic analyzer captures prefetches, even if they are not executed. When you are specifying a trigger condition or a storage qualification that follows an instruction that may cause branching, an unused prefetch may generate an unwanted trigger.

### No activity on activity indicators

- Check for loose cables, board connections, and analysis probe interface connections.
  - Check for bent or damaged pins on the analysis probe.
- 

### No trace list display

If there is no trace list display, it may be that your trigger specification is not correct for the data you want to capture, or that the trace memory is only partially filled.

- Check your trigger sequencer specification to ensure that it will capture the events of interest.
  - Try stopping the analyzer; if the trace list is partially filled, this should display the contents of trace memory.
- 

### Analyzer won't power up

If logic analyzer power is cycled when the logic analyzer is connected to a target system or emulation probe that remains powered up, the logic analyzer may not be able to power up. Some logic analyzers are inhibited from powering up when they are connected to a target system or emulation probe that is already powered up.

- Disconnect all logic analyzer cabling from the analysis probe. This will allow the logic analyzer to power up. Reconnect logic analyzer cabling after power up.

## Analysis Probe Problems

This section lists problems that you might encounter when using an analysis probe. If the solutions suggested here do not correct the problem, you may have a damaged analysis probe. Contact your local Agilent Technologies Sales Office if you need further assistance.

---

### Target system will not boot up

If the target system will not boot up after connecting the analysis probe interface, the microprocessor (if socketed) or the analysis probe interface may not be installed properly, or they may not be making electrical contact.

- Ensure that you are following the correct power-on sequence for the analysis probe and target system.

- 1 Power up the analyzer and analysis probe.
- 2 Power up the target system.

If you power up the target system before you power up the analysis probe, interface circuitry in the analysis probe may latch up and prevent proper target system operation.

- Verify that the microprocessor and the analysis probe interface are properly rotated and aligned, so that the index pin on the microprocessor (pin A1) matches the index pin on the analysis probe interface.
- Verify that the microprocessor and the analysis probe interface are securely inserted into their respective sockets.
- Verify that the logic analyzer cables are in the proper sockets of the analysis probe interface and are firmly inserted.

## Erratic trace measurements

- Do a full reset of the target system before beginning the measurement.  
Some analysis probe designs require a full reset to ensure correct configuration.
- Ensure that your target system meets the timing requirements of the processor with the analysis probe installed.  
See “Capacitive loading” in this chapter. While analysis probe loading is slight, pin protectors, extenders, and adapters may increase it to unacceptable levels. If the target system design has close timing margins, such loading may cause incorrect processor functioning and give erratic trace results.
- Ensure that you have sufficient cooling for the microprocessor.  
Ensure that you have ambient temperature conditions and airflow that meet or exceed the requirements of the microprocessor manufacturer.

---

## Capacitive loading

Excessive capacitive loading can degrade signals, resulting in incorrect capture by the analysis probe interface, or system lockup in the microprocessor. All analysis probe interfaces add additional capacitive loading, as can custom probe fixtures you design for your application.

Careful layout of your target system can minimize loading problems and result in better margins for your design. This is especially important for systems that are running at frequencies greater than 50 MHz.

- Remove as many pin protectors, extenders, and adapters as possible.
- If multiple analysis probe interface solutions are available, use one with lower capacitive loading.



## State Analysis Problems

This section lists problems that you might encounter while using the B3759A #710 emulation solution user interface software.

When you obtain incorrect inverse assembly results, it may be unclear whether the problem is in the analysis probe or in your target system. If you follow the suggestions in this section to ensure that you are using the analysis probe and inverse assembler correctly, you can proceed with confidence in debugging your target system.

---

### No inverse assembly or incorrect inverse assembly

This problem may be due to incorrect synchronization, modified configuration, incorrect connections, or a hardware problem in the target system. A locked status line can cause incorrect or incomplete inverse assembly.

- Ensure that each logic analyzer pod is connected to the correct analysis probe connector.

There is not always a one-to-one correspondence between analyzer pod numbers and analysis probe cable numbers. Analysis Probes must supply address (ADDR), data (DATA), and status (STAT) information to the analyzer in a predefined order. The cable connections for each analysis probe are often altered to support that need. Thus, one analysis probe might require that you connect cable 2 to analyzer pod 2, while another will require you to connect cable 5 to analyzer pod 2. See Chapter 3 for connection information.

- Check the activity indicators for status lines locked in a high or low state.
- Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values.

These labels must remain as they are configured by the configuration file. Do not change the names of these labels or the bit assignments within the labels. Some analysis probes also require other data labels. See Chapter 3 for more information.

- Verify that all microprocessor caches have been disabled.

In most cases, if the microprocessor caches remain enabled you should still get inverse assembly. It may be incorrect because a portion of the execution trace was not visible to the logic analyzer.

Chapter 8: Troubleshooting the Analysis Probe  
**State Analysis Problems**

- Verify that storage qualification has not excluded storage of all the needed opcodes and operands.

## Intermodule Measurement Problems

Some problems occur only when you are trying to make a measurement involving multiple modules.

---

### An event wasn't captured by one of the modules

If you are trying to capture an event that occurs very shortly after the event that arms one of the measurement modules, it may be missed due to internal analyzer delays. For example, suppose you set an oscilloscope module to trigger upon receiving a trigger signal from the logic analyzer because you are trying to capture a pulse that occurs right after the analyzer's trigger state. If the pulse occurs too soon after the analyzer's trigger state, the oscilloscope will miss the pulse.

- Adjust the skew in the Intermodule menu.

You may be able to specify a skew value that enables the event to be captured.

- Change the trigger specification for modules upstream of the one with the problem.

If you are using a logic analyzer to trigger an oscilloscope module, try specifying a trigger state one state before the one you are using. This may be more difficult than working with the skew because the prior state may occur more often and not always be related to the event you are trying to capture with the oscilloscope.

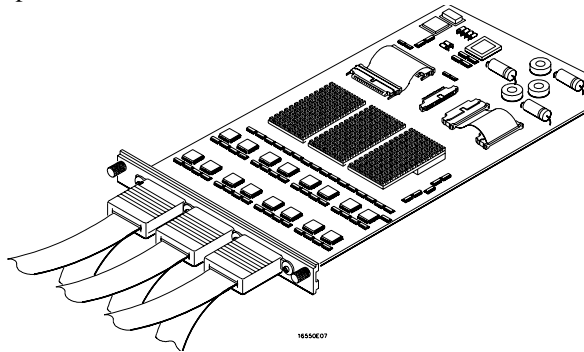
## Analysis Probe Messages

This section lists some of the messages that the analyzer displays when it encounters a problem.

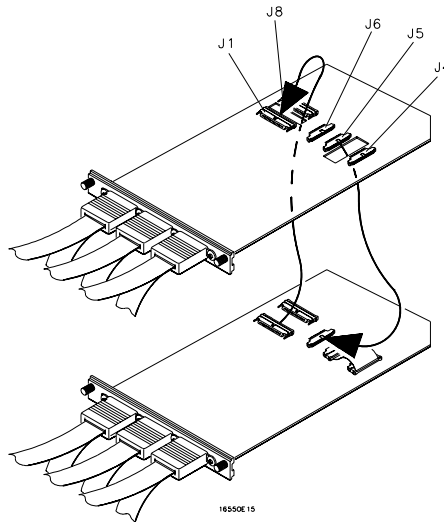
---

### “Measurement Initialization Error”

This error occurs when you have installed the cables incorrectly for one or two Agilent Technologies 16550A logic analysis cards. The following diagrams show the correct cable connections for one-card and two-card installations. Ensure that your cable connections match the silk screening on the card, and that they are fully seated in the connectors. Then, repeat the measurement.



**Cable Connections for One-Card Agilent Technologies 16550A Installations**



**Cable Connections for Two-Card Agilent Technologies 16550A Installations**

**See Also**

*The Agilent Technologies 16550A 100-MHz State/500-MHz Timing Logic Analyzer Service Guide.*

### “No Configuration File Loaded”

This is usually caused by trying to load a configuration file for one type of module/system into a different type of module/system.

- Verify that the appropriate module has been selected from the Load {module} from File {filename} in the disk operation menu. Selecting Load {All} will cause incorrect operation when loading most analysis probe interface configuration files.

**See Also**

Chapter 2 describes how to load configuration files.

---

### “Selected File is Incompatible”

This occurs when you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

---

### “Slow or Missing Clock”

- This error message might occur if the logic analyzer cards are not firmly seated in the logic analysis system frame. Ensure that the cards are firmly seated.
- This error might occur if the target system is not running properly. Ensure that the target system is on and operating properly.
- If the error message persists, check that the logic analyzer pods are connected to the proper connectors on the analysis probe interface. See Chapter 2 to determine the proper connections.

### “Time from Arm Greater Than 41.93 ms”

The Agilent Technologies 16550A state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

---

### “Waiting for Trigger”

If a trigger pattern is specified, this message indicates that the specified trigger pattern has not occurred. Verify that the triggering pattern is correctly set.

- When analyzing microprocessors that fetch only from word-aligned addresses, ensure that the trigger condition is set to look for an opcode fetch at an address corresponding to a word boundary,

## Returning Parts to Agilent Technologies for Service

The repair strategy for this emulation solution is board replacement.

Exchange assemblies are available when a repairable assembly is returned to Agilent Technologies. These assemblies have been set up on the "Exchange Assembly" program. This lets you exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

---

### To return a part to Agilent Technologies

- 1 Follow the procedures in this chapter to make sure that the problem is caused by a hardware failure, not by configuration or cabling problems.
- 2 Call your nearest Agilent Technologies sales office. Ask them for the address of the nearest Agilent Technologies service center.
- 3 Package the part and send it to the Agilent Technologies service center.  
Keep any parts which you know are working. For example, if only the target interface module is broken, keep the emulation module and cables.
- 4 When the part has been replaced, it will be sent back to you.  
The unit returned to you will have the same serial number as the unit you sent to Agilent Technologies.



## To obtain replacement parts

The following table lists some parts that may be replaced if they are damaged or lost. Contact your nearest Agilent Technologies Sales Office for further information.

### Analysis Probe Replaceable Parts

<b>Agilent Part Number</b>	<b>Description</b>
E5346A	High-density Cable
E8029-66501	Analysis Probe Circuit Board
E5350-23801	Cam Tool
E5322-60001	Retainer Kit
E5322-23801	Locator Tool
E5374A	208 pin QFP Elastomeric Probe

---

## Cleaning the Instrument

If the instrument requires cleaning:

- 1** Remove power from the instrument.
- 2** Clean the instrument with a mild detergent and water.
- 3** Make sure that the instrument is completely dry before reconnecting it to a power source.

Chapter 8: Troubleshooting the Analysis Probe  
**Cleaning the Instrument**

---

## Troubleshooting the Emulation Module

---

## Troubleshooting the Emulation Module

If you have problems with the emulation module, your first task is to determine the source of the problem. Problems may originate in any of the following places:

- The connection between the emulation module and your debugger
- The emulation module itself
- The connection between the emulation module and the Trace Port Analyzer
- The connection between the Trace Port Analyzer and the Target interface module
- The connection between the target interface module and the target system
- The target system

You can use several means to determine the source of the problem:

- The troubleshooting guide on the next page
- The status lights on the emulation probe or emulation module
- The emulator "performance verification" tests
- The Trace Port Analyzer "performance verification" tests
- The emulator's built-in "terminal interface" commands

---

## Emulation Module Troubleshooting Guide

---

### Common problems and what to do about them

Symptom	What to do	See also
Commands from debugger have no effect	Your debugger may not be configured properly. If this does not work, continue with the steps for the next symptom....	page 111
Emulation module built-in commands do not work	<p><b>1</b> Run the emulation module performance verification tests.</p> <p><b>2</b> If the performance verification tests pass, then there is an electrical problem with the connection to the target processor OR the target system may not have been designed according to "Designing a Target System."</p>	page 120 page 68, page 114
"Slow or missing clock" message after a logic analyzer run	Check that the target system is running user code or is in reset. (This message can appear if the processor is in background mode.)	
Host computer reports LAN connection problems	Follow the checklist in the "If you have LAN problems" section.	page 118
Commands from the Run Control tool or debugger have no effect	Verify LAN communication.	page 111

## Status Lights

### Emulation Module Status Lights

The emulation module uses status lights to communicate various modes and error conditions.

The following table gives more information about the meaning of the power and target status lights.

- = LED is off
- = LED is on
- \* = Not applicable (LED is off or on)

---

### Power/Target Status Lights

---

Pwr/Target LEDs	Meaning
<input type="radio"/> Reset <input type="radio"/> Break <input type="radio"/> Run	No target system power, or emulation module is not connected to the target system
<input checked="" type="radio"/> Reset <input type="radio"/> Break <input type="radio"/> Run	Target system is in a reset state
<input type="radio"/> Reset <input checked="" type="radio"/> Break <input type="radio"/> Run	The target processor is executing in Debug Mode
<input type="radio"/> Reset <input type="radio"/> Break <input checked="" type="radio"/> Run	The target processor is executing user code
<input type="radio"/> Reset <input checked="" type="radio"/> Break <input checked="" type="radio"/> Run	Only boot firmware is good (other firmware has been corrupted)

## Emulation Module Built-in Commands

The emulation module has some built-in "terminal interface" commands which you can use for troubleshooting. You can access the terminal interface using:

- A telnet (LAN) connection
- A "debugger command" window in your debugger

---

### To telnet to the emulation module

You can establish a telnet connection to the emulation module if:

- A host computer and the logic analysis system are both connected to a local-area network (LAN), and
- The host computer has the telnet program (often part of the operating system or an internet software package).

To establish a telnet connection:

- 1** Find out the port number of the emulation module.

The default port number of the first emulation module in an Agilent Technologies 16600A/700A series logic analysis system is 6472. The default port of a second module in an Agilent Technologies 16600A-series system is 6476. The default port numbers of a third and fourth module in an expansion frame are 6480 and 6484. These port numbers can be changed, but that is rarely necessary.

- 2** Find out the LAN address or LAN name of the logic analysis system.
- 3** Start the telnet program.

If the LAN name of the logic analysis system is "test2" and you have only one emulation module installed, the command might look like this:

```
telnet test2 6472
```

- 4** If you do not see a prompt, press the <Return> key a few times.

To exit from this telnet session, type <CTRL>D at the prompt.

## To use the built-in commands

Here are a few commonly used built-in commands:

---

### Useful built-in commands

---

b	Break -- go into the background monitor state
cf	Configuration -- read or write configuration options
help	Help -- display online help for built-in commands
init	Initialize -- init -c re-initializes everything in the emulation module except for the LAN software; init -p is the equivalent of cycling power (it will break LAN connections)
lan	configure LAN address
m	Memory -- read or write memory
reg	Register -- read or write a register
r	Run -- start running user code
rep	Repeat -- repeat a command or group of commands
rst	Reset -- reset the target processor (the emulation module will wait for you to press the target's RESET button)
s	Step -- do a low-level single step
ver	Version -- display the product number and firmware version of the emulation module



The prompt indicates the status of the emulation module:

---

**Emulation module prompts**

---

U	Running user program
M	Running in background monitor
p	No target power
R	Emulation reset
r	Target reset
?	Unknown state

---

**Examples**

To set register R0, then view R0 to verify that it was set, enter:

```
R>rst -m  
M>reg r0=ffff  
M>reg r0  
   reg R0=0000ffff
```

To break execution then step a single instruction, enter:

```
M>b  
M>s  
   PC=xxxxxxxx  
M>
```

To determine what firmware version is installed in the emulation module, enter:

```
M>ver
```

---

**See Also**

Use the `help` command for more information on these and other commands. Note that some of commands listed in the help screens are generic commands for Agilent Technologies emulators and may not be available for your product.

If you are writing your own debugger, contact Agilent Technologies for more information.

## Problems with the Target System

This section describes how to determine whether your target system is causing problems with the operation of the emulation module.

---

### What to check first

- 1 Try some basic built-in commands using the Command Line window or a telnet connection:

```
U>rst  
R>
```

This should reset the target and display a "R>" prompt.

```
R>b  
M>
```

This should stop the target and display an "M>" prompt.

```
M>reg r1  
    reg r1=00000000  
M>
```

This should read the value of the r1 register (the value will probably be different on your target system).

```
M>m 0..  
00000000  7c3043a6 7c2802a6 7c3143a6 4bf04111  
00000010  00000000 00000000 00000000 00000000  
00000020  00000000 00000000 00000000 00000000  
00000030  00000000 00000000 00000000 00000000  
00000040  00000000 00000000 00000000 00000000  
00000050  00000000 00000000 00000000 00000000  
00000060  00000000 00000000 00000000 00000000  
00000070  00000000 00000000 00000000 00000000  
M>
```

This should display memory values starting at address 0.

```
M>s
```

This should execute one instruction at the current program counter.

If any of these commands don't work, there may be a problem with the design of your target system, a problem with the revision of the emulation you are using, or a problem with the configuration of the emulation module. The following steps will help you identify the problem.

- 2 Check that the emulation module firmware matches your processor. To do this, enter:

```
M>>ver
```

**See Also**

Page 111 for information on entering built-in commands.

## To interpret the initial prompt

The initial prompt can be used to diagnose several common problems. To get the most information from the prompt, follow this procedure:

Connect the emulation module to your target system.

Make sure that your target system is turned off.

Set the default configuration settings. Enter:

```
M>init -c
```

### **If the response is "!ERROR 905! Driver firmware is incompatible with ID of attached device"**

Make sure the target interface module is connected to the cable of the emulation module, then try the "init -c" command again.

When you enter the command, the prompt should be showing either "?>" or "p>".

Please follow the steps below.

- 1 If the prompt shows "?>", you must turn the target system's power off and turn it back on. When the target power is turned on, the prompt should show "R>".
- 2 If the prompt shows "p>", you must turn the target system's power on. When the target power is turned on, the prompt should show "R>".
- 3 If the prompt still shows either "p>" or "?>" after executing the above steps, check the voltage of the pin 8 of the Hitachi-UDI debug port. The voltage should be same as the target  $V_{DD}$  (normally 3.0V).
- 4 When you see the "R>" prompt, enter the following command:

```
R>b
```

The prompt should show "M>". If the prompt does not change to "M>", check the processor's /TRST signal. The signal should be driven to high for the proper operation.

- 5 If the prompt does not show "M>" after executing the above step, check the Hitachi-UDI clock speed. The speed should be slower than the processor's internal module clock speed. You may change the clock speed by entering the following command.

```
R>cf speed=CLOCK(1-7)
```

You must choose the CLOCK speed from the following

- 1 => 10.5MHz
  - 2 => 5.25MHz
  - 3 => 2.63MHz
  - 4 => 1.32MHz
  - 5 => 0.656MHz
  - 6 => 0.328MHz
  - 7 => 0.164MHz
- 6** Turn the target power off and turn it back on. Repeat the steps 3 through 5.

## Problems with the LAN Interface

---

### If LAN communication does not work

If you cannot verify connection using the procedure in "To verify LAN communication", or if the commands are not accepted by the emulation module:

- Make sure that you wait for the power-on self test to complete before connecting.
- Make sure that the LAN cable is connected. Watch the LAN LED's on the back of the logic analysis system to see whether the system is seeing LAN activity. Refer to your LAN documentation for testing connectivity.
- Check that the host computer or debugger was configured with the correct LAN address. If the logic analysis system is on a different subnet than the host computer, check that the gateway address is correct.
- Make sure that the logic analysis system's IP address is set up correctly.

## If it takes a long time to connect to the network

- ❑ Check the subnet masks on the other LAN devices connected to your network. All of the devices should be configured to use the same subnet mask.

Subnet mask error messages do not indicate a major problem. You can continue using the emulation module.

The subnet mask is set in the logic analysis system's System Admin window. If it then detects other subnet masks, it will generate error messages.

If there are many subnet masks in use on the local subnet, the logic analysis system may take a very long time to connect to the network after it is turned on.

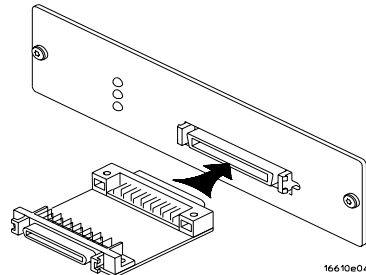
## Problems with the Emulation Module

Occasionally you may suspect a hardware problem with the emulation module or target interface module. The procedures in this section describe how to test the hardware, and if a problem is found, how to repair or replace the broken component.

---

### To run the built-in performance verification test using the logic analysis system (emulation module only)

- 1 End any Emulation Control Interface or debugger sessions.
- 2 Disconnect the 50-pin cable from the emulation module, and plug the loopback test board (Agilent part number E3496-66502) into the emulation module.



- 3 In the system window, click the emulation module and select **Performance Verification**.
- 4 Click **Start PV**.  
The results will appear on screen.



---

## To run complete performance verification tests using a telnet connection (emulation module only)

- 1 Disconnect the 50-pin cable from the emulation module, and plug the loopback test board (Agilent part number E3496-66502) directly into the emulation module. Do not plug anything into the other end of the loopback test board.  
On a good system, the RESET LED will light and the BKG and USER LEDs will be out.
- 2 telnet to the emulation module.
- 3 Enter the **pv 1** command.

**See Also** Options available for the "pv" command are explained in the help screen displayed by typing "help pv" or "? pv" at the prompt. Note, however, that some of the options listed may not apply to your emulation module.

---

**Examples:** If you are using a UNIX system, to telnet to a logic analysis system named "mylogic", enter:

```
telnet mylogic 6472
```

Here are some examples of ways to use the **pv** command.

To execute both tests one time:

```
pv 1
```

To execute test 2 with maximum debug output repeatedly until a ^C is entered:

```
pv -t2 -v9 0
```

To execute tests 3, 4, and 5 only for 2 cycles:

```
pv -t3-5 2
```

The results on a good system with the loopback test board connected, are as follows:

```
M>pv 1
```

```
Testing: E3499C Series Emulation System
Test 1: Powerup PV Results                Passed!
Test 2: Target Probe Feedback Test        Passed!
Test 3: Boundary Scan Master Test         Passed!
Test 4: I2C Test                          Passed!
Test 5: Data Lines Test                   Passed!
PASSED Number of tests: 1                 Number of failures: 0
```

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Chapter 9: Troubleshooting the Emulation Module  
**Problems with the Emulation Module**

E3499C Series Emulation System  
Version: A.07.51 17Dec97  
Location: Generics

E3467A Hitachi SH7750 Emulator  
Version: A.01.00

M>

### If a performance verification test fails

- Details of the failure can be obtained through using a -v option ("verbose" level) of 2 or more.
- Check that the loopback test board is connected.
- If the problem persists, contact Agilent Technologies for assistance.

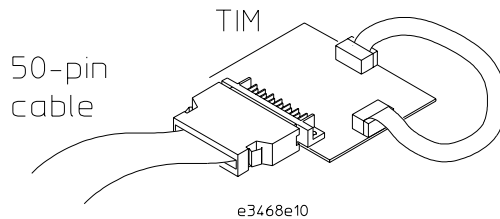
---

## Problem with the TIM

---

To perform the TIM only PV tests with an emulation probe/module

- 1 End any Emulation Control Interface or debugger sessions.
- 2 Plug the 14-pin cable to the loop-back connector of the TIM.



- 3 Telnet to the emulation probe/module.
- 4 Enter **pv 1** command.

The result will appear on screen as below.

```
Testing: E3499B Series Emulation System
  Test  1: Powerup PV Results                Passed!
  Test  2: LAN 10Base2 Feedback Test         Not Executed!
  Test  3: LAN 10BaseT Feedback Test         Not Executed!
  Test  4: Break In and Trigger Out BNC Feedback Test Passed!
  Test  5: Target Probe Feedback Test        Not Executed!
  Test  6: Boundary Scan Master Test         Not Executed!
  Test  7: I2C Test                          Not Executed!
  Test  8: Data Lines Test                   Passed!
Testing: E3467A Hitachi SH7750 Series Emulator
  Test  1: TIM Test                          Passed!
PASSED  Number of tests: 1                    Number of failures: 0
```

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```
E3499B Series Emulation System
Version:  A.07.07 06Jul98 12:56
Location:  Generics
```

E3467A Hitachi SH7750 Emulator  
Version: A.01.00

Details of the failure can be obtained through using a -v option ("verbose" level) of 2 or more.

- Check that the loopback test board is connected.
- If the problem persists, contact Agilent Technologies for assistance.

## Returning Parts to Agilent Technologies for Service

The repair strategy for this emulation solution is board replacement.

Exchange assemblies are available when a repairable assembly is returned to Agilent Technologies. These assemblies have been set up on the "Exchange Assembly" program. This lets you exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

---

### To return a part to Agilent Technologies

- 1** Follow the procedures in this chapter to make sure that the problem is caused by a hardware failure, not by configuration or cabling problems.
- 2** In the U.S., call 1-800-403-0801. Outside the U.S., call your nearest Agilent Technologies sales office. Ask them for the address of the nearest Agilent Technologies service center.
- 3** Package the part and send it to the Agilent Technologies service center.  
Keep any parts which you know are working. For example, if only the target interface module is broken, keep the emulation module and cables.
- 4** When the part has been replaced, it will be sent back to you.  
The unit returned to you will have the same serial number as the unit you sent to Agilent Technologies.

The Agilent Technologies service center can also troubleshoot the hardware and replace the failed part. To do this, send your entire measurement system to the service center, including the logic analysis system, target interface module, and cables.

In some parts of the world, on-site repair service is available. Ask an Agilent Technologies sales or service representative for details.

## To obtain replacement parts

The following table lists some parts that may be replaced if they are damaged or lost. The part numbers are subject to change. Contact your nearest Agilent Technologies Sales Office for further information.

---

### Part numbers

---

#### Exchange Assemblies

Part Number	Description
16600-69515	Emulation module

#### Replacement Assemblies

Part Number	Description
E3467-61601	14-pin target cable
E3496-61601	50-pin cable
E3496-66502	Loopback test board
E3467-66501	Target Interface Module
16700-61608	Expansion cable for emulation module

## Cleaning the Instrument

If the instrument requires cleaning:

- 1 Remove power from the instrument.
- 2 Clean the instrument with a mild detergent and water.
- 3 Make sure that the instrument is completely dry before reconnecting it to a power source.



---

## Glossary

**Analysis Probe**

A probing solution connected to the target microprocessor. It provides an interface between the signals of the target microprocessor and the inputs of the logic analyzer. Formerly called a "preprocessor."

**Elastomeric Probe Adapter**

A connector that is fastened on top of a target microprocessor using a retainer and knurled nut. The conductive elastomer on the bottom of the probe adapter makes contact with pins of the target microprocessor and delivers their signals to connection points on top of the probe adapter.

**Emulation Module**

An emulation module is installed within the mainframe of a logic analyzer. It provides run control within an emulation and analysis test setup. See Emulation Probe.

**Emulation Probe**

An emulation probe is a standalone instrument connected to the mainframe of a logic analyzer. It provides run control within an emulation and analysis test setup. Formerly called a

"processor probe" or "software probe." See Emulation Module.

**Extender**

A part whose only function is to provide connections from one location to another. One or more extenders might be stacked to raise a probe above a target microprocessor to avoid mechanical contact with other components installed close to the target microprocessor. Sometimes called a "connector board."

**Flexible Adapter**

Two connection devices coupled with a flexible cable. Used for connecting probing hardware on the target microprocessor to the analysis probe.

**General-Purpose Flexible Adapter**

A cable assembly that connects the signals from an elastomeric probe adapter to an analysis probe. Normally, a male-to-male header or transition board makes the connections from the general-purpose flexible adapter to the analysis probe.

**High-Density Adapter Cable**

A cable assembly that delivers signals from an analysis probe hardware

## Glossary

interface to the logic analyzer pod cables. A high-density adapter cable has a single Mictor connector that is installed into the analysis probe, and two cables that are connected to corresponding odd and even logic analyzer pod cables.

### **High-Density Termination Adapter Cable**

Same as a High-Density Adapter Cable, except it has a termination in the Mictor connector.

### **Jumper**

Moveable direct electrical connection between two points.

### **Mainframe Logic Analyzer**

A logic analyzer that resides on one or more board assemblies installed in an Agilent Technologies 16500, 1660x, or 16600A/700A-series mainframe.

### **Male-to-male Header**

A board assembly that makes point-to-point connections between the female pins of a flexible adapter or transition board and the female pins of an analysis probe.

### **Preprocessor**

See Analysis Probe.

### **Preprocessor Interface**

See Analysis Probe.

### **Probe adapter**

See Elastomeric Probe Adapter.

### **Processor Probe**

See Emulation Probe.

### **Prototype Analyzer**

The Agilent Technologies 16505A prototype analyzer acts as an analysis and display processor for the Agilent Technologies 16500B/C logic analysis system. It provides a windowed interface and powerful analysis capabilities. Replaced by Agilent Technologies 16600A/700A-series logic analysis systems.

### **Run Control Probe**

See Emulation Probe and Emulation Module.

### **Setup Assistant**

A software program that guides a user through the process of connecting and configuring a logic analyzer to make measurements on a specific microprocessor.

### **Shunt Connector.**

See Jumper.

### **Software Probe**

See Emulation Probe.

### **Solution**

Agilent Technologies' term for a set of tools for debugging your target system. A solution includes probing, inverse assembly, the Agilent Technologies B4620B Source Correlation Tool Set, and possibly an emulation module.

**Stand-alone Logic Analyzer**

A standalone logic analyzer has a predefined set of hardware components which provide a specific set of capabilities. It is designed to perform logic analysis. A standalone logic analyzer differs from a mainframe logic analyzer in that it does not offer card slots for installation of additional capabilities, and its specifications are not modified based upon selection from a set of optional hardware boards that might be installed within its frame.

**Target Control Port**

An 8-bit, TTL port on a logic analysis system that you can use to send signals to your target system. It does not function like a pattern generator or emulation module, but more like a remote control for the target's switches.

**Target Interface Module**

A small circuit board which connects the 50-pin cable from an emulation module or emulation probe to signals from the debug port on a target system.

**TIM**

See Target Interface Module.

**Trace Port Analyzer**

A small logic analyzer which was specialized for PC-Trace function dedicated in Tx19/39 series processors.

**Trigger Specification**

A set of conditions that must be true before the instrument triggers. See the

printed or online documentation for your logic analyzer for details.

**Transition Board**

A board assembly that obtains signals connected to one side and rearranges them in a different order for delivery at the other side of the board.

**1/4-Flexible Adapter**

An adapter that obtains one-quarter of the signals from an elastomeric probe adapter (one side of a target microprocessor) and makes them available for probing.

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---

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# DECLARATION OF CONFORMITY

according to ISO/IEC Guide 22 and EN 45014

**Manufacturer's Name:** Agilent Technologies  
**Manufacturer's Address:** Digital Design Product Generation Unit  
1900 Garden of the Gods Road  
Colorado Springs, CO 80907 USA

declares, that the product

**Product Name:** Logic Analyzer Mainframe  
**Model Number(s):** Agilent Technologies 16700A  
**Product Option(s):** All

conforms to the following Product Specifications:

**Safety:** IEC 1010-1:1990+A1 / EN 61010-1:1993  
UL3111  
CSA-C22.2 No. 1010.1:1993

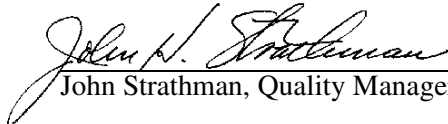
**EMC:** CISPR 11:1990 / EN 55011:1991                      Group 1 Class A  
IEC 555-2:1982 + A1:1985 / EN 60555-2:1987  
IEC 555-3:1982 + A1:1990 / EN 60555-3:1987 + A1:1991  
IEC 801-2:1991 / EN 50082-1:1992                      4 kV CD, 8 kV AD  
IEC 801-3:1984 / EN 50082-1:1992                      3 V/m, {1kHz 80% AM, 27-1000 MHz}  
IEC 801-4:1998 / EN 50082-1:1992                      0.5 kV Sig. Lines, 1 kV Power Lines

## Supplementary Information:

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This product was tested in a typical configuration with Agilent Technologies test systems.

Colorado Springs, 09/22/97

  
John Strathman, Quality Manager

European Contact: Your local Agilent Technologies Sales and Service Office or Agilent Technologies GmbH, Department ZQ / Standards Europe, Herrenberger Strasse 130, D-71034 Böblingen Germany (FAX: +49-7031-14-3143)

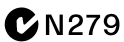
## Product Regulations

**Safety** IEC 1010-1:1990+A1 / EN 61010-1:1993  
UL3111  
CSA-C22.2 No. 1010.1:1993

**EMC** This Product meets the requirement of the European Communities (EC) EMC Directive 89/336/EEC.



**Emissions** EN55011/CISPR 11 (ISM, Group 1, Class A equipment),  
IEC 555-2 and IEC 555-3



<b>Immunity</b>		Code <sup>1</sup>	Notes <sup>2</sup>
EN50082-1			
IEC 801-2 (ESD) 4kV CD, 8kV AD		3	
IEC 801-3 (Rad.) 3 V/m		1	
IEC 801-4 (EFT) 0.5 kV, 1kV		3	

<sup>1</sup>Performance Codes:

1 PASS - Normal operation, no effect.

2 PASS - Temporary degradation, self recoverable.

3 PASS - Temporary degradation, operator intervention required.

4 FAIL - Not recoverable, component damage.

<sup>2</sup>Notes: (none)

**Sound Pressure Level** Less than 60 dBA



# DECLARATION OF CONFORMITY

according to ISO/IEC Guide 22 and EN 45014

**Manufacturer's Name:** Agilent Technologies  
**Manufacturer's Address:** Digital Design Product Generation Unit  
1900 Garden of the Gods Road  
Colorado Springs, CO 80907 USA

declares, that the product

**Product Name:** Logic Analyzer  
**Model Number(s):** Agilent Technologies 16600A, 16601A, 16602A,  
16603A  
**Product Option(s):** All

conforms to the following Product Specifications:

**Safety:** IEC 1010-1:1990+A1 / EN 61010-1:1993  
UL3111  
CSA-C22.2 No. 1010.1:1993

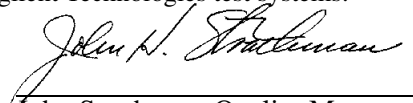
**EMC:** CISPR 11:1990 / EN 55011:1991 Group 1 Class A  
IEC 555-2:1982 + A1:1985 / EN 60555-2:1987  
IEC 555-3:1982 + A1:1990 / EN 60555-3:1987 + A1:1991  
IEC 801-2:1991 / EN 50082-1:1992 4 kV CD, 8 kV AD  
IEC 801-3:1984 / EN 50082-1:1992 3 V/m, { 1kHz 80% AM, 27-1000 MHz }  
IEC 801-4:1998 / EN 50082-1:1992 0.5 kV Sig. Lines, 1 kV Power Lines

## Supplementary Information:

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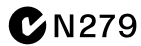
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**Safety** IEC 1010-1:1990+A1 / EN 61010-1:1993  
UL3111  
CSA-C22.2 No. 1010.1:1993

**EMC** This Product meets the requirement of the European Communities (EC) EMC Directive 89/336/EEC.



**Emissions** EN55011/CISPR 11 (ISM, Group 1, Class A equipment),  
IEC 555-1 and IEC 555-2



<b>Immunity</b>	EN50082-1	Code <sup>1</sup>	Notes <sup>2</sup>
	IEC 801-2 (ESD) 4kV CD, 8kV AD	3	1
	IEC 801-3 (Rad.) 3 V/m	3	
	IEC 801-4 (EFT) 0.5 kV, 1kV		

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1 PASS - Normal operation, no effect.

2 PASS - Temporary degradation, self recoverable.

3 PASS - Temporary degradation, operator intervention required.

4 FAIL - Not recoverable, component damage.

<sup>2</sup>Notes: (none)

**Sound Pressure Level** Less than 60 dBA

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• This apparatus has been designed and tested in accordance with IEC Publication 1010, Safety Requirements for Measuring Apparatus, and has been supplied in a safe condition. This is a Safety Class I instrument (provided with terminal for protective earthing). Before applying power, verify that the correct safety precautions are taken (see the following warnings). In addition, note the external markings on the instrument that are described under "Safety Symbols."

#### Warning

- Before turning on the instrument, you must connect the protective earth terminal of the instrument to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. You must not negate the protective action by using an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
- Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short-circuited fuseholders. To do so could cause a shock or fire hazard.

- Service instructions are for trained service personnel. To avoid dangerous electric shock, do not perform any service unless qualified to do so. Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.
- If you energize this instrument by an auto transformer (for voltage reduction), make sure the common terminal is connected to the earth terminal of the power source.
- Whenever it is likely that the ground protection is impaired, you must make the instrument inoperative and secure it against any unintended operation.
- Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.
- Do not install substitute parts or perform any unauthorized modification to the instrument.
- Capacitors inside the instrument may retain a charge even if the instrument is disconnected from its source of supply.
- Use caution when exposing or handling the CRT. Handling or replacing the CRT shall be done only by qualified maintenance personnel.

#### Safety Symbols



Instruction manual symbol: the product is marked with this symbol when it is necessary for you to refer to the instruction manual in order to protect against damage to the product.



Hazardous voltage symbol.



Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis.

#### WARNING

The Warning sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a Warning sign until the indicated conditions are fully understood and met.

#### CAUTION

The Caution sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a Caution symbol until the indicated conditions are fully understood or met.

### **Product Warranty**

This Agilent Technologies product has a warranty against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Agilent Technologies Company will, at its option, either repair or replace products that prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by Agilent Technologies.

For products returned to Agilent Technologies for warranty service, the Buyer shall prepay shipping charges to Agilent Technologies and Agilent Technologies shall pay shipping charges to return the product to the Buyer. However, the Buyer shall pay all shipping charges, duties, and taxes for products returned to Agilent Technologies from another country.

Agilent Technologies warrants that its software and firmware designated by Agilent Technologies for use with an instrument will execute its programming instructions when properly installed on that instrument. Agilent Technologies does not warrant that the operation of the instrument software, or firmware will be uninterrupted or error free.

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### **Certification**

Agilent Technologies certifies that this product met its published specifications at the time of shipment from the factory. Agilent Technologies further certifies that its calibration measurements are traceable to the United States National Institute of Standards and Technology, to the extent allowed by the Institute's calibration facility, and to the calibration facilities of other International Standards Organization members.

### **About this edition**

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